A New Approach towards Embedded Logic in a Single Device

Sehtab Hossain[1], Md Arif Iqbal, Mostafizur Rahman[2]
Computer Science Electrical Engineering, University of Missouri-Kansas City, MO, USA
shgf4@mail.umkc.edu[1], rahmanmo@umkc.edu[2]

***Abstract*— With the scaling limitations of traditional FETs, the new device and circuit concepts have emerged to continue miniaturization of ICs. Previously, we proposed a new circuit paradigm, called Crosstalk logic, where interference between adjacent wires was leveraged to compute logic. In this paper, we present a new approach towards realizing Crosstalk logic behavior in a single device. This approach revolves around the manipulation of device parameters and usage of independent gates in devices like planar double-gate FET to achieve desired Crosstalk logic. Our investigation with a 25nm gate length device validates the assumptions. In this brief, we show AND logic behavior in a single device, and correlate it with Crosstalk design principles. Such device design approaches could open up new possibilities in denser circuit design and ultimately benefit technology scaling.**

Keywords*— *Crosstalk Computing, Planar Double Gate FinFET, TCAD

I. INTRODUCTION

As traditional IC scaling is reaching fundamental limits [1-5], embedding logic in a single device by manipulating device parameters provides alternative pathways [6]. However, a systematic approach is missing towards achieving hierarchical circuits and complex logic functions. We propose a novel approach to solve this problem, implementing a standalone device to perform embedded logic.

Our approach towards embedded logic in a device starts with the premise of a new computing paradigm, called Crosstalk computing [7-14]. In Crosstalk Computing, interference between adjacent metal lines is engineered to achieve a particular logic behavior. Metal lines, coupling capacitance, and synchronous clock are key components in Crosstalk Computing. The narrowly spaced metal lines will experience interference when a signal transition takes place. The strength of the coupling capacitance relies on the sum of coupling capacitance induced in both metal wires. We have shown that this inference-based computing paradigm can be used to implement a variety of gates including custom and configurable ones, and also shown pathways to build larger circuits [14].

To capture Crosstalk logic behavior in a single device, we have implemented a Planar Double Gate FinFET with 25nm gate length using Technology Computer-Aided Design (TCAD) Sprocess. We have characterized the device in SDevice. The device has I_{on} of 500e-6 A/μm and $I_{off.}$ of 3.76e-13 A/μm, the threshold voltage of 0.59 V, Subthreshold Swing (SS) of 62 mV/dec and Drain Induced Barrier Lowering (DIBL) of 25 mV/V from I-V plot.

Several key parameters like device dimensions, gate oxide thickness, material work function are manipulated to required interference between the aggressor to achieve the Crosstalk logic. In this paper, we have shown AND gate behavior using the Crosstalk concept in the standalone device. We have also shown that by varying oxide thickness and work function, the device characteristics can be tuned to get different logic functionality.

The rest of the paper is arranged as follows: Section II discusses the Crosstalk aspects and how Crosstalk comes into account. Section III discusses the modeling approach of the device along with geometric parameters and proper process steps and physical computation. Device characteristics and other crucial device physics effects are presented elaborately here. Section IV presents the results. Finally, Section V concludes the paper.

II. CROSSTALK DESIGN FUNDAMENTALS

An abstract view of Crosstalk fabric is presented in Fig. 1.i). The key components of Crosstalk computing are: a) metal nano-lines and their logic specific arrangements to drive inputs, b) engineered coupling capacitance between these lines, and c) synchronous clock inputs and one transistor-based scheme to control the output behavior. Fig. 1ii shows primitive gate designs. At a particular clock period, the output node (called 'victim') is kept floating, and inputs are transitioned from 1to 0 or 0 to 1 in the surrounding input metal lines (called 'aggressors'). As a result of transitions in aggressors, the summation of aggressor charges gets induced in the victim node through capacitive coupling (Fig. 1.ii). The magnitude of the induced signal depends on the coupling capacitance value. The coupling capacitance is inversely proportional to the separation of metal lines and directly proportional to the permittivity of the dielectric and lateral area of metal lines. Tuning the coupling capacitance values using its variables provides the engineering freedom to tailor the induced summation signal to a specific logic implementation.

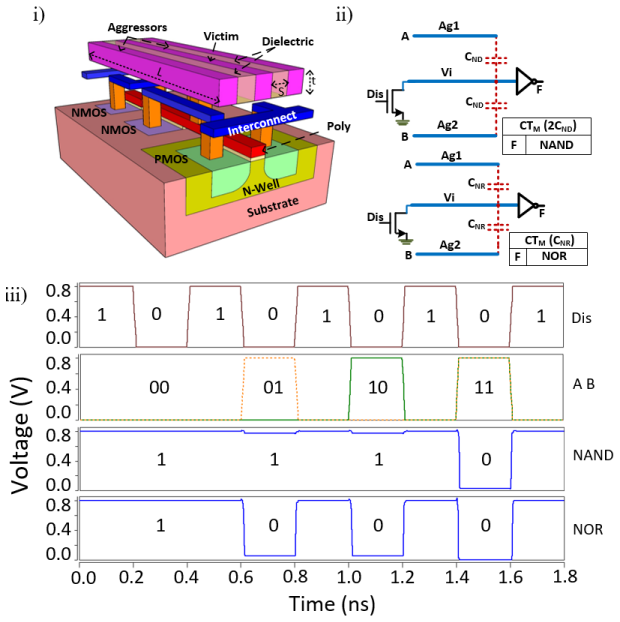

Fig. 1. i) Abstract view of Crosstalk computing Fabric; coupling capacitances will be on the top denoted as 'dielectric' in between nano-metal lines denoted as 'aggressors' and 'victim'. ii) Schematic of primitive cells (NAND & NOR) in Crosstalk fabric. Inputs will be given through metal lines and coupled with Vi line for logic computation, iii) Simulation results of Crosstalk NAND and NOR gate.

To control the victim's floating behavior and to ensure synchronization, a transistor is used (Figs. 1ii), which is gated by a discharge ('dis') signal. After every computation, the dis signal will be turned ON to discharge the floating node. In Figs. 1i and 1ii, we show the implementation of NAND and NOR gates in Crosstalk fabric. Both implementations require three transistors and have identical layouts with the only difference of coupling capacitance strength. NOR gate's (Fig. 1ii) coupling C_{NR} is stronger than NAND gate's (Fig. 1ii) coupling C_{ND}. The Crosstalk circuit style is fundamentally different from CMOS, where each transistor is gated with input, and the output transitions when the input changes.

As a result of transistor switching, the output node gets connected to a static VDD/GND signal. In contrast, Crosstalk computing is dynamic; the output node is kept floating by disconnecting it from GND through a switched off transistor, and when the input transitions in *A* and/or *B* occurs, charges are induced in the *OUT* node (Fig. 1iii). The inverters connected to *vi*-nodes ensure the full swing output. Since NAND/NOR constitute universal logic, any logic function can be implemented with Crosstalk. In later sections, we will show how we are achieving these functionalities in a single device by meticulously engineering the device and material parameters.

III. Modeling Approach of the Single Device

Our device modeling approach accounts Crosstalk computing concept. In our simulation approach, we have implemented the device first and then characterized it using 3-D TCAD process and device simulation.

In the Sentaurus process simulator, the device structure is created by emulating the actual process flow. The process parameters (e.g., implantation dosage, anneal temperature, etc.) used in this simulation is given in Table I. Fig. 2.i depicts our process-simulated device where Gate-1 and Gate-2 are independent gates in a double-gated device. Gate and contact materials labeled in the figure are chosen-based on work-function requirements for achieving the aggressor-victim like scenario. Additionally, coupling capacitance plays a key role in Crosstalk technology [9]. Material work function and gate oxide thickness of the device are investigated to achieve the required interference to implement the logic. Our process simulation starts with wafer preparation. The wafer plane of (100) is selected and then Silicon-On-Insulator (SOI) wafer with (100) Miller Plane is formed. Advanced calibration is chosen to get the fine mesh of 1 nm. For gate material, we have selected Titanium Nitride (TiN) with a work function of 4.7 eV and for gate oxide, Hafnium Oxide (HfO_2) with 1nm thickness is chosen to form high-k/metal gate formation. Then Phosphorus implantation is performed which leads to a doping concentration of 6e18cm^{-3}. Table I. depicts all the geometric parameters of the device.

Table I: Device Geometry

Technology Parameters	Value
Gate Length (nm)	25
Fin Diameter (nm)	5
Gate Oxide Thickness (nm)	1
S/D Length (nm)	50
S/D Doping (cm^{-3})	5e18
Channel Doping (cm^{-3})	1e16
Channel Stop Doping (cm^{-3})	1e14

Then, for characterizing the device behavior, process simulated structure is used in TCAD device simulation. To get the device characteristics, we have included doping dependence mobility to get ON current. High field saturation for velocity saturation is also taken into account. The channel doping and other device parameters used in device simulation to compare drive current at 0.7V drain bias. To observe OFF current behavior, the Oldslotboom model is included in the computation. A fully coupled or 'Newton' method for the self-consistent solution of the Poisson and electron continuity equation is specified. Fig. 2.ii depicts the I-V characteristics of the device obtained from the device simulation. The device has I_{on} of 500e-6A/µm and I_{off} of 3.76e-13A/µm, Subthreshold Swing (SS) of 62mV/dec, and Drain Induced Barrier Lowering (DIBL) of 25mV/V. The threshold voltage of the device is 0.59V with Mid bandgap metal of TiN as gate metal which has a work function of 4.6 eV. Source and drain doping are 5e18cm^3.

IV. Result and Discussion

We have implemented a 2-input AND gate using Crosstalk technology in the single device explained above. We have also shown that the key device parameters like work function or oxide thickness can be tuned to obtain the desired logic behavior.

In Crosstalk technology, coupling capacitance plays a key role in achieving the logic behavior which inversely proportional to the separation of metal lines and directly proportional to the permittivity of the dielectric and lateral

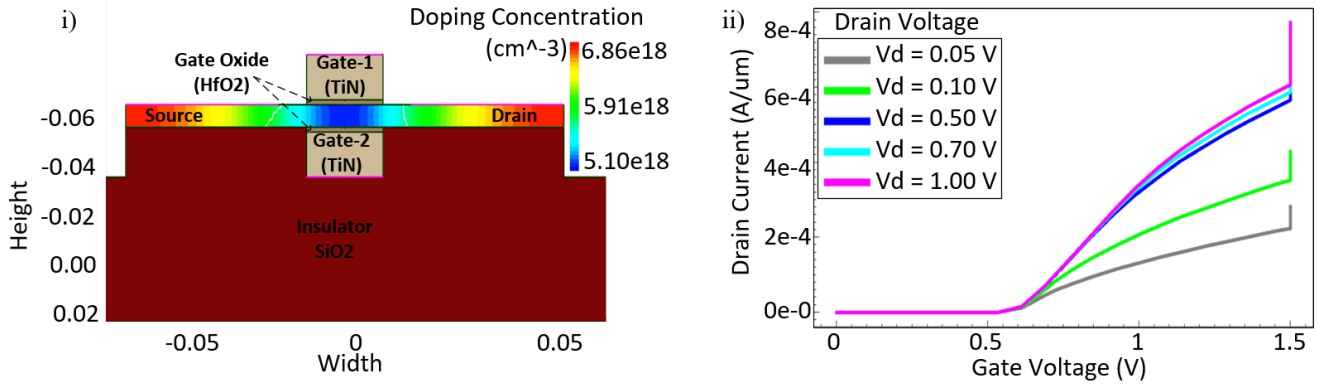

Fig 2. Device structure and characteristics of a Planar Double Gate FET. i) Process emulated device structure; the device has gate length of 25 nm, channel thickness of 5 nm, and HfO2 as gate oxide with thickness of 1 nm between both gates. n+ concentration is 6e18 cm-3, ii) I-V characteristics of the Planar DG FET. The device has threshold voltage of 0.53 V, I_{off} = 3.76e-13 A/µm and I_{on} = 500e-6 A/µm

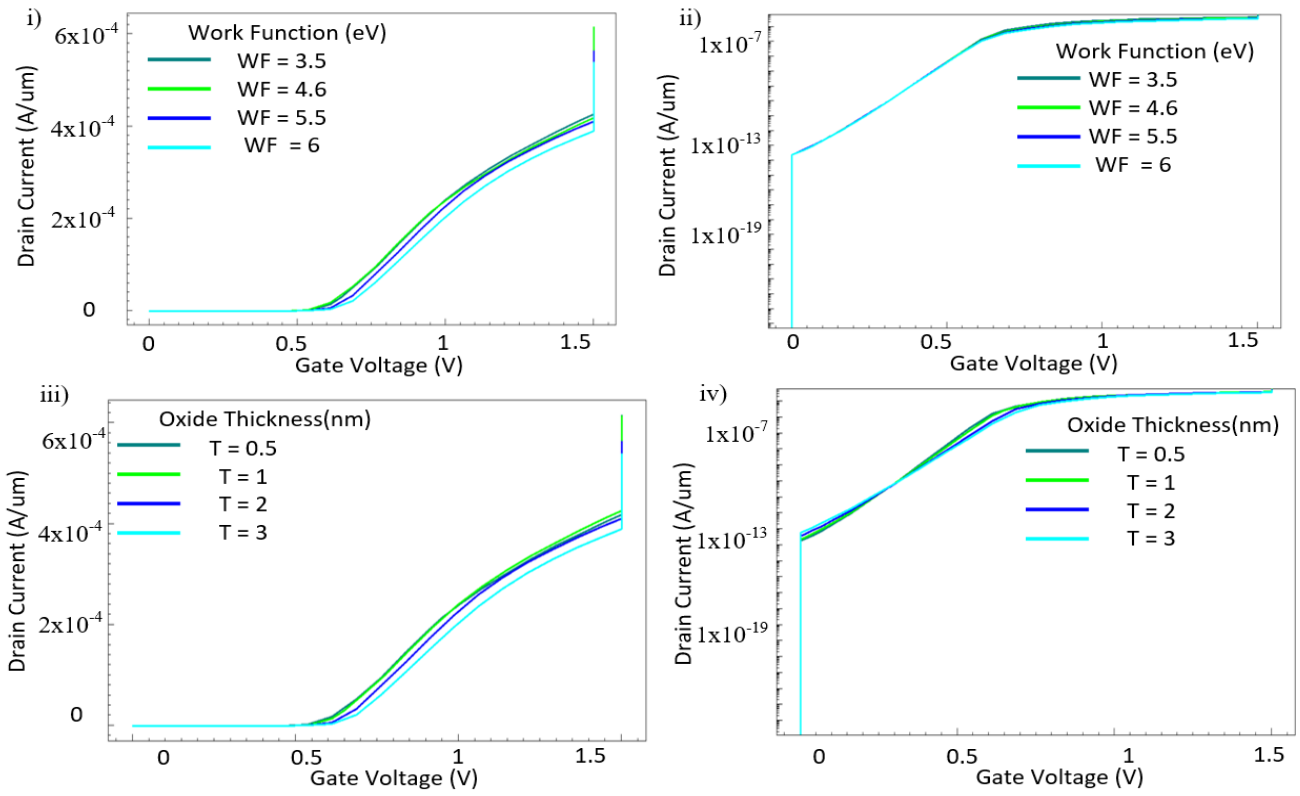

Fig. 3. Impact of varying work function and Oxide thickness on Gate current i) Gate-1 I-V with varying work function ii) Log plot of I-V for Gate-1 iii) Gate-1 I-V varying gate oxide thickness iv) Log plot of I-V for Gate-1 varying oxide thickness

area of metal lines. For this case, we have investigated the impact gate oxide thickness and work function on the gate current. In Fig. 3i&ii, we have shown the impact of work function in the I-V characteristics of the device. Fig. 3i shows the liner plot and Fig. 3ii shows a log plot where we can see that the device reaches the saturation. The work function is strongly related to flat band voltage and threshold voltage and also influences the ON-current and OFF-current. From Fig. 3.i, it can be seen that the maximum ON current can be achieved for the work function of 3.1eV. The ON current is low for other work functions because of the increase in the potential barrier and threshold voltage as the value of work function increases. We have also varied the oxide thickness and examined the impact of it on the I-V characteristics. For a very thin oxide layer, ON current starts decreasing as the gate loses electrostatic control and short channel effect becomes prominent. However, for other thickness values, with the different logic states, ON-current shows a linear relation. From Fig. 3.iii and iv it can be seen the for oxide thickness of both the 0.5nm and 1nm the ON current is maximum. For any other case, it should remain below the threshold.

We have emulated the Crosstalk 2-input AND gate in the single device described above. To implement the AND behavior Crosstalk behavior, the induced voltage at the victim line should be above threshold during voltage transition in both the gates. It is important to However, to achieve the Crosstalk behavior in the device, at first we have done extensive investigation on the impact of varying work functions on the gate. Fig. 4.i shows 2-input AND behavior. The inputs are given through Gate-1 and Gate-2. It is noticed

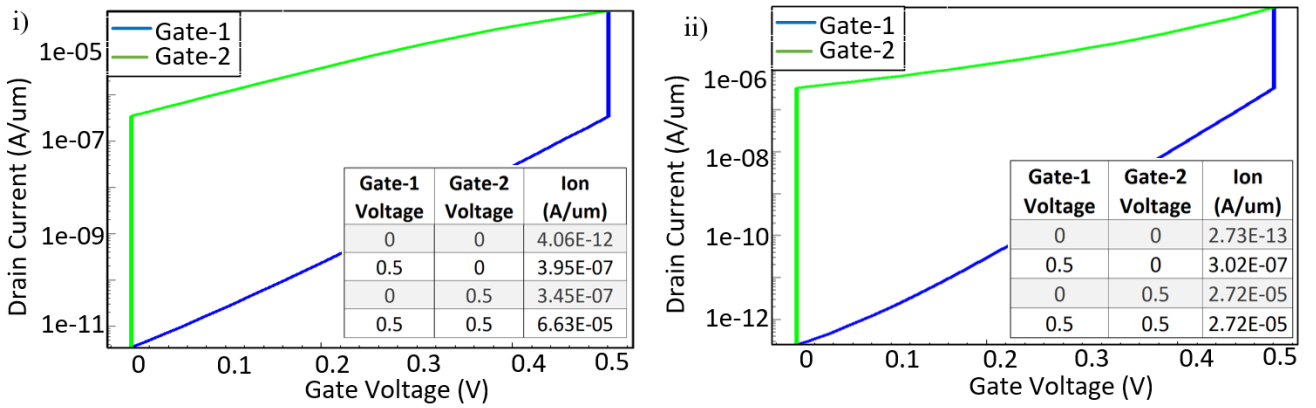

Fig. 4. Crosstak behavior in the proposed device. i) Same gate oxide thickness at Gate-1 and Gate-2; When both gates are at 0.5 V, they will obtain I_{on} and exhibits AND behavior, ii) Different gate oxide thickness at Gate-1 and Gate-2; Gate-2 gate oxide thickness is 30 A˚ as such exhibits dominant behavior as shown in the table.

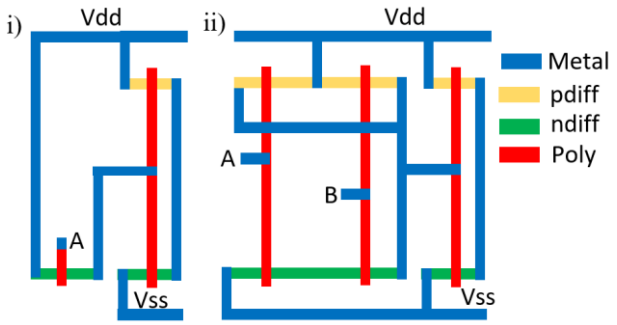

Fig. 5. Layout of AND gate. i) Layout using proposed embedded logic in a single device ii) Layout using traditional CMOS device our proposed device's area is 3x time smaller than traditional CMOS area.

that the device offers a maximum current of 6.63e-05 A/µm when both gates receive input voltage. For any other logic cases, the current is significantly low which is below the threshold limit (also shown in the inset table of Fig. 4.i) which infer the behavior of an AND gate. A different Crosstalk behavior is also implemented in the device and shown in Fig. 4.ii. By varying the coupling strength, we can increase the weight of any gate to achieve different complex Boolean functions like (AB+C). As shown in Fig. 4.ii, the ON-Current characteristics are indicative of a bias towards Gate-2.

Achieving such Crosstalk logic behavior in a single device is indicative of denser circuit design. Many such density benefits can be found in [16], for example, the full adder circuit, CMOS implementation requires 40 transistors in cascaded topology (12 transistors for each XOR gates and 12 for carrying logic), whereas the Crosstalk implementation requires just 13 and the interconnection requirements are also considerably less. As can be seen from the layout of an AND in Fig. 5. The AND gate is 3x smaller compared to CMOS counterpart irrespective of the technology node.

V. CONCLUSION

Crosstalk Logic is a very novel and radically different way of doing logic computation. In this paper, we have shown a new way of realizing the Crosstalk logic behavior in a single device. The paper presents a detailed framework for achieving device structure and characteristics. Our proposed device successfully implemented the AND logic. We have also shown the methodology of achieving different functionality by using the proposed device. Such a standalone device design approach provides huge density benefits and hence an alternative solution to IC scaling.

REFERENCES

[1] Fischetti, M. V., et al. "Scaling MOSFETs to 10 nm: Coulomb effects, source starvation, and virtual source model." *Journal of computational electronics* 8.2 (2009): 60-77.

[2] E. Pop, "Energy dissipation and transport in nanoscale devices," Nano Res., vol. 3, no. 3, pp. 147–169, 2010.

[3] Y.-B. Kim, "Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics," Trans. Electr. Electron. Mater., vol. 11, no. 3, pp. 93–105, 2010.

[4] K. J. Kuhn, "CMOS transistor scaling past 32nm and implications on variation," ASMC (Advanced Semicond. Manuf. Conf. Proc., vol. 97124, pp. 241–246, 2010.

[5] D. Vasileska, K. Raleva, and S. M. Goodnick, "Heating Effects in Nanoscale Devices," Cut. Edge Nanotechnol., no. Ic, pp. 43–69, 2010.

[6] Liu, Y. X., et al. "4-terminal FinFETs with high threshold voltage controllability." Conference Digest Device Research Conference, 2004. 62nd DRC. IEEE, 2004.

[7] Naveen kumar Macha, et al.,"A New Concept for Computing using Interconnect Crosstalks," IEEE International Conference on Rebooting Computing (ICRC),Washington, DC, 2017, pp. 1-2.

[8] M. A. Iqbal, et.al.,"A Logic Simplification Approach for Very Large Scale Crosstalk Circuit Designs," IEEE/ACM Symposium on Nanoscale Architectures,2019.

[9] Macha, Naveen Kumar, et al. "A New Paradigm for Fault-Tolerant Computing with Interconnect Crosstalks." 2018 IEEE International Conference on Rebooting Computing (ICRC). IEEE, 2018.

[10] Macha, Naveen, et al. "Crosstalk based Fine-Grained Reconfiguration Techniques for Polymorphic Circuits." Proceedings of the 14th IEEE/ACM International Symposium on Nanoscale Architectures. 2018.

[11] Macha, N. K., et al. "A New Paradigm for Computing for Digital Electronics under Extreme Environments." 2019 IEEE Aerospace and Electronic Systems Society, Big Sky. 2019.

[12] M. A. Iqbal, et.al, "Design and Comparison of Crosstalk Circuits at 7nm," IEEE Conference on Rebooting Computing,2019

[13] Naveen Kumar Macha, Sandeep Geedipally, Bhavana Repalle, M. A. Iqbal, Wafi Danesh, Mostafizur Rahman ,"Crosstalk based Fine-Grained Reconfiguration Techniques for Polymorphic Circuits," IEEE/ACM International Symposium on Nanoscale Architectures,2018

[14] Naveen kumar Macha, Bhavana Tejaswini Repalle, Sandeep Geedipally, Rafael Rios, Mostafizur Rahman "A New Paradigm for Fault-Tolerant Computing with Interconnect Crosstalks," 2018 IEEE International Conference on Rebooting Computing (ICRC), Washington, DC, USA, December 2018

[15] Nowak, Edward J., et al. "Turning silicon on its edge [double gate CMOS/FinFET technology]." IEEE Circuits and Devices Magazine 20.1 (2004): 20-31.

[16] Hadia, Sarman K., Rohit R. Patel, and Yogesh P. Kosta. "FinFET architecture analysis and fabrication mechanism." International Journal of Computer Science Issues (IJCSI) 8.5 (2011): 235.

[17] Tripathi, S. L., Ramanuj Mishra, and R. A. Mishra. "Characteristic comparison of connected DG FINFET, TG FINFET and Independent Gate FINFET on 32 nm technology." 2012 2nd International Conference on Power, Control and Embedded Systems. IEEE, 2012.

[18] Liu, Yongxun, et al. "Investigation of the TiN gate electrode with tunable work function and its application for FinFET fabrication." IEEE transactions on nanotechnology 5.6 (2006): 723-730.

[19] Chowdhury, Murshed M., et al. "Carrier mobility/transport in undoped-UTB DG FinFETs." IEEE transactions on electron devices 54.5 (2007): 1125-1131.

[20] M. A. Iqbal, et.al., "From 180nm to 7nm: Crosstalk Computing Scalability Study," IEEE Electron Device Society S3S Conference,2019.