Designing Crosstalk Circuits at 7nm

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Abstract*— Crosstalk is an innovative computing technology that utilizes unwanted interferences between interconnects to compute useful logic. Engineering of coupling capacitance, circuit scheme and integration are core features. This paper presents scalability aspects of Crosstalk technology to compete/co-exist with CMOS for digital logic implementations below 10nm. Scalability is a key requirement for any emerging technologies to continue chip miniaturization. Our scalability study is with Arizona State Predictive (ASAP) 7nm PDK and considers all process variation aspects. We present primitive gate designs and their performance under variations. We discuss design constraints to accommodate worst-case variation scenarios. Finally, utilizing primitive gates, we show larger designs such as cm85a, mux, and pcle from MCNC benchmarking suits and detailed comparison with CMOS at 7nm. Our benchmarking revealed, averaging all three above mentioned circuits, 48%, 57% and 10% improvements against CMOS designs in terms of transistor count, power and performance respectively.

Keywords—Crosstalk Computing, Large-scale Circuit Design, Process Variation, ASAP 7nm PDK

I. Introduction

Crosstalk computing provides a scalable alternative solution to CMOS while leveraging CMOS devices and interconnect technologies [1]-[5]. In Crosstalk computing, interference between the metal lines at advanced technology nodes is engineered in an efficient manner to obtain logic functions. Nano metal lines are placed in a compact manner so that whenever signal transitions take place in one of the lines the sum of their Crosstalk interference gets induced in another metal line through coupling capacitance. The strength of the coupling capacitance determines how the charge is going to be induced on the victim metal line and thereby can be engineered to obtain different logic functions. The key components of the Crosstalk computing fabric are metal lines, coupling capacitances, a synchronous clock, and inverter. The coupling capacitances between aggressors and the victim are inversely proportional to the separation of metal lines and directly proportional to the permittivity of the dielectric and lateral area of metal lines, which can be engineered according to required logic function.

Like any other emerging technology, scalability study is also a key requirement for Crosstalk computing. However, to completely assess the effectiveness of new design methodologies at advanced technology node, a standard process design kit (PDK) with the full set of collateral necessary for schematic entry, layout, design rule checking, parasitic extraction, transistor-level simulation, library generation, synthesis, and automatic placement and routing (APR) is required.

In this paper, we do scalability study with Arizona State Predictive 7nm PDK (ASAP7) [7]. ASAP7 PDK comes with predictive technology models for transistors and design collaterals including libraries and technology files that are required by the CAD tools. Through worst-case process variation analysis, we demonstrate that even at sub 10nm, Crosstalk logic gates function properly. Using these primitive logic gates, we designed larger circuits like cm85a, mux, and pcle from MCNC benchmark suit [8] and compared the results with CMOS at 7nm. Our comparison results show 59%, 62% and 23% reduction in transistor count for cm85a. mux and pcle circuits, respectively. Our simulation results also show potentials for power and performance improvements; in average for the three circuits, reduction in power and performance was 57% and 10%.

The rest of the paper is organized as follows. Section II discusses scalability and Crosstalk Computing Concept and presents implementations of basic logic circuits. Section III discusses the impact of process variation in Crosstalk Computing at 7nm. The behavior of Crosstalk NAND and NOR gate for different process corners is also shown here. Section IV explains the design aspects for larger-scale using Crosstalk logic cells at 7nm. Section V gives the benchmarking results. Finally, Section VI concludes the paper.

II. Scaling Challenges & Crosstalk Design Aspects

Scalability is a major concern for CMOS, and in order for any emerging technologies to compete/co-exist with CMOS the scalability litmus test need to be passed. For CMOS, the scaling has been driven by shrinking transistors first, and challenges are mainly due to the reduction in transistor drive strength, manufacturability and interconnection overhead. Crosstalk computing, utilizing CMOS transistors and processes, proposes an alternative paradigm which puts emphasis on circuit design and integration first. Our benchmarking shows that through design 2-5x density benefits are possible over CMOS with improved power at a same node. Although the prospects are promising, one may question how variability and signal integrity challenges can be passed by a technology that relies on noise. To answer this question, we first discuss Crosstalk's computing aspects and then detail design constraints.

Fig.1 shows the example of two primitive cells (NAND & NOR) constructed in Crosstalk fabric. In any logic cell, the underlying principle is to emulate the behavior of aggressor-victim commonly found in interconnects. During logic computation, the victim net (*Vi*) voltage is controlled electrostatically through coupling capacitances between two aggressors (*Ag1* and *Ag2*) and victim (*Vi*) net. To drive the *Vi* node for next round of logic evaluation, its voltage is discharged to ground through a transistor controlled by *dis* signal after every round of logic evaluation. The *dis* signal also ensures synchronization with the rest of the circuits. Thus, the *Vi* node is connected to an inverter on one end and connected to the drain side of the discharge transistor on the other end. After every computation, the *dis* signal will be turned ON to discharge the *Vi* node. Initially, the *Vi* node is kept floating at 0 (because of the previous discharge cycle), and when the input transitions in *A* and *B* occurs, output summation charge is induced on *Vi*, which in turn drives the inverter acting as a threshold function. This same principle is used while implementing both NAND and NOR gates with the only difference of coupling strengths between inputs and *Vi* net. For NOR gate, the coupling (C_{NR}) is stronger than NAND gates (C_{ND}) and is chosen such that whenever any of the inputs

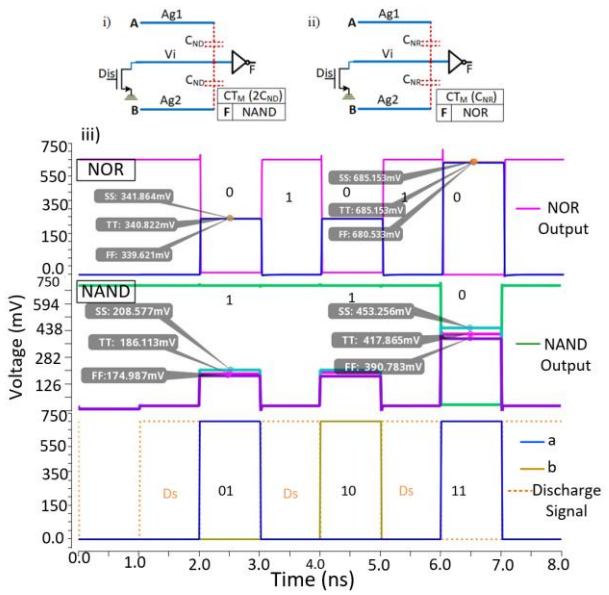

Fig.1 Fundamental Logic Gates: i) NAND ii) NOR iii) Simulation results of NAND and NOR gate with *Vi* node voltage under different process variation

or both the inputs transition (A or B), the *Vi* node gets the summation voltage 1 (the inverter output receives 0, hence NOR gate). For NAND, both the inputs need to transition to 1 to receive the summation voltage 1 on *Vi* node (0 at F). HSPICE simulation results validate the Crosstalk principles (Fig.2 (iii)). The inverter connected to *Vi* make the logic inverted and ensures full swings for fan-outs. The inverter is one of the key components of the Crosstalk fabric that acts as a threshold function which regenerates the signals and restores them to full swing. Fig.1iii also shows that even though process variations has impact on the victim node voltage (Vi) but CT logic circuits are still able to maintain the functionality by achieving proper output. As discussed in the previous section, if the *Vi* node voltage goes below the switching threshold voltage of 0.3V, the inverter will output logic level '0' and vice versa. Such low switching threshold voltage of the inverter is indeed a key parameter since for any instance, if the output voltage does not achieve full swing, the inverter will still be able to respond incoming voltage.

As mentioned, Crosstalk computing fundamentally relies on interference between nodes for compute. However, transistors play an important role in controlling the interference pattern and ensuring full swing output. Therefore, transistor related variability challenges persists in Crosstalk, but the overall effect is lesser due to the less number of transistors being used.

III. Designing Under Variation at 7nm

Process variation may arise due to various issues and ultimately impact transistor performance, hence the standard in the industry is to name different process corners as FF (Fast-Fast), TT (Typical-Typical) and SS (Slow-Slow) with the first letter refers to NMOS and later one refers to PMOS. By combining FS, FT, etc., other process corners can be obtained; however, FF, TT and SS are representative of best, nominal and worst case scenarios. Fig. 2 shows the effect of process variation on the transfer characteristics curve of an unskewed inverter at 7nm. As can be seen from the Fig. 2, the inverter has a weak PMOS transistor causing the switching threshold (*Vm*) to shift more towards zero. In general, the switching threshold voltage is desirable to be equal to exactly half of VDD (0.35V) since this would provide higher noise margin. For worst- case process variation (SS), *Vm* moves more towards left (Fig. 2) and thereby, increases the undefined region. Under such condition, any incoming signal with noisy zero value would lead to erroneous values at the output.

For Crosstalk computing, with symmetrical inverter connected to its *Vi* node, the incoming input value, as can be seen from the Fig. 2, should lie within 0V to 0.33V to have perfect logic '1' at the inverter output. However, to have better noise immunity and balanced drive strength, the width of the PMOS needs to be increased since this would shift the switching voltage towards half of the VDD. The properties obtained from Fig. 2 from different process corner is very useful for designing Crosstalk circuits with different fan-ins and indicative of power and performance profile.

We used the ASAP7nm PDK [7] to evaluate Crosstalk circuits at 7nm. ASAP7 PDK is compatible with industry CAD tools for full physical verification (Layout design, DRC, PEX, and LVS). The PDK is a 7nm FinFET technology that comes with transistor models having four different threshold voltage levels. The four devices reported in ASAP7 PDK are SLVT, LVT, RVT, and SRAM in decreasing order of drive strength, for both NMOS and PMOS transistors. The RVT type NMOS transistor has Ion of 37.85uA and Ioff of 0.019uA, providing excellent subthreshold swing of 63.03 mV/decade. Similarly, PMOS transistor also has a similar subthreshold swing of 64.48 mV/decade having Ion of 32.88uA and Ioff 0.023uA. Using these NMOS and PMOS transistor, for an unskewed inverter, high noise margin is found to be 0.33V and low noise margin to be 0.3V with switching threshold voltage at 0.34V.

Fig. 3(i&ii) shows the power and performance results of Crosstalk NAND and NOR gate at three process corners for PMOS and NMOS devices: SS, TT and FF. As shown in Fig. 3i&ii, the slow transistors result in a slower transition of 5.53ps and 8.77ps for both NAND and NOR gate, respectively, but the functionality remains intact. The delay is minimum for the FF corner, but the power is also highest. The bar graphs show the impact of process variation on performance and power for both NAND and NOR gate with TT being the nominal case.

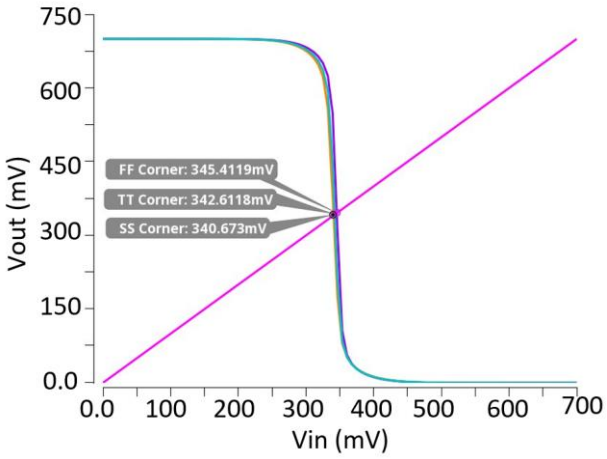

Fig. 2 Voltage characteristics curve of an Inverter for different process variation

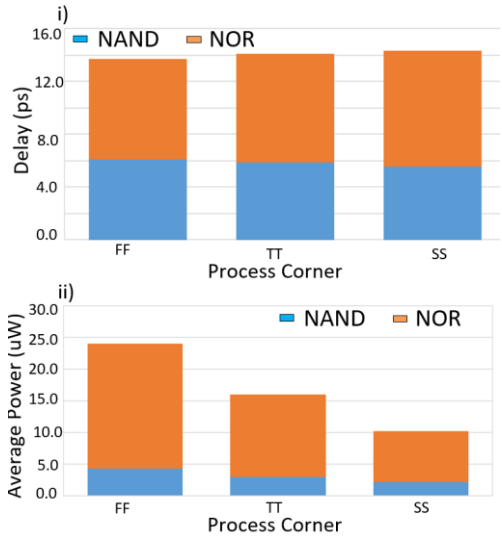

Fig. 3 Impact of process variation on i) Performance and ii) Average power for CT NAND and NOR Gate

IV. Designing Large-Scale Circuits In Crosstalk Technology

Different Crosstalk primitive logic cells can be achieved using the methodology explained in earlier and also shown in [2]. These Crosstalk cells can be connected in a cascaded manner for large-scale circuit design.

Fig. 4 shows an example of a large circuit implementation using Crosstalk computing and Fig. 5 shows the simulation results of the circuit. The circuit is 'cm85a' circuit, one of the

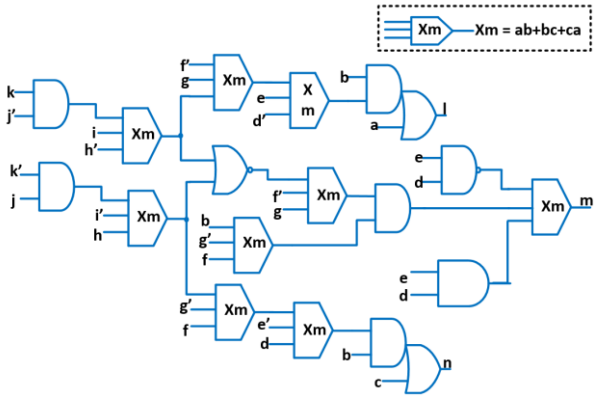

Fig. 4. Schematic of cm85a circuit

benchmarking circuits from MCNC suits [8]. The circuit has eleven primary inputs (a-k) and three primary outputs (l-n) as shown in Fig. 4. The netlist of the circuit is obtained from the MCNC and then further simplified to get Crosstalk friendly netlist according to the process explained in [11]. More benefits can be achieved when the Crosstalk circuits is implemented in homogeneous ($f= ab+bc+ca$) or heterogeneous manner ($f=a+bc$) [11].

Implementing large circuits using Crosstalk gates, requires attention on maintaining signal integrity and drive strength for the next stage gates. These issues can be addressed by adding inverter at the end of the victim node. The inverter acts as a thresholding function that is if the victim node voltage is below a certain voltage limit, the inverter restores the logic level '0' and vice versa. The strength of the inverter depends

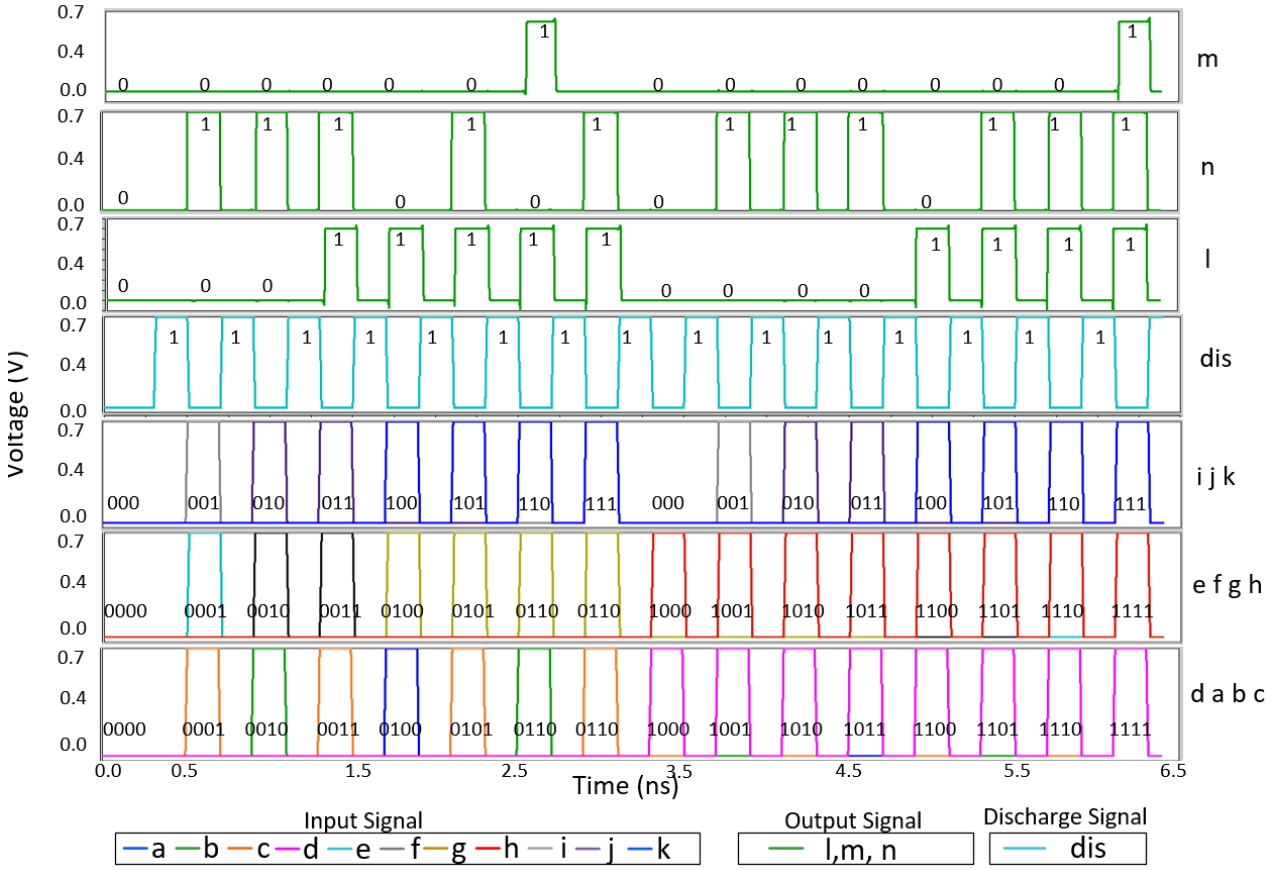

Fig. 5. Simulation results of cm85a circuit design at 7nm

TABLE I. COMPARISON OF DENSITY, POWER AND PERFROMASION FOR DIFFERENT LARGE-SCALE CIRCUIT

MCNC Benchmark Circuits	I/O		Transistor Count			Average Power (uW)			Performance (ps)		
	CMOS	*Crosstalk*	*CMOS*	*Crosstalk*	*%Reduction*	*CMOS*	*Crosstalk*	*%Reduction*	*CMOS*	*Crosstalk*	*%Reduction*
NAND2	2/1	2/1	4	3	25	0.119	0.075	37	7.78	5.79	25.57
NOR2	2/1	2/1	4	3	25	0.376	0.387	-3	6.56	8.22	-25.3
Cm85a	11/3	11/3	168	69	59.00	60.63	28.95	52.25	21.10	18.93	10.28
Mux	21/1	21/1	506	190	62.45	73.70	29.90	59.43	9.43	12.75	-35.2
Pcle	19/9	19/9	328	252	23.17	288	110	61.80	15.04	7.07	53.00

on the number of fan-out load or type of Crosstalk gates, it is driving. As can be seen in Fig. 4, at the second level, Crosstalk gates are driving two fan-out loads of higher coupling capacitances. To avoid the signal drop at the fan-in of the next stage gates, the inverters are designed as hi-skewed inverter. Another key issue, specific to Crosstalk circuit, is during each evaluation state, the CT gates need a transition of the input signal from 0 to 1 for correct logic operation. So, if a logic high is retained on the victim node from the previous operation, it leads to logic failure. For example, in Fig. 4, at third level, a CT-NOR gate, which is an inverting CT-logic gate, is driving the next stage CT-homogenous gate. During discharge (Dis) state, it receives a logic high which is carried to the next evaluation state and thereby prevents the transition of signal from 0 to 1 leading to logic failure. This issue can be resolved by using a pass-gate type circuit style [2]. In this type of circuit style, a transmission gate is placed between an inverting and non-inverting gate interfaces. During discharge state, input signal coming from the aggressor that is connected to the transmission-gate is discharged to ground and in evaluation state, the input signal is passed through the transmission-gates thus, creating a signal transition from 0 to 1. For CT-circuits with three inputs, especially for CT-OR3 gates, high coupling strength is required for proper logic function. This is due to the case that the victim node requires more charge accumulation to turn on the inverter connected to it, the inverter has a higher threshold voltage. However, since ASAP7 PDK, comes with transistor models with four different threshold voltages, the transistor that requires lower threshold voltage can be used in CT-OR3 gates to avoid higher coupling. Additionally, buffers can be used to maintain the signal strength to drive the gates that are far placed. Using the above-mentioned steps, the cm85a circuit is implemented and simulation results in Fig. 5 shows the correct functionality is maintained. As such, any large-scale circuits can be implemented using CT-gates in this manner while maintaining correct circuit functionality and achieving improved density, power and performance benefits.

V. Comparison and Benchmarking

Table I shows the detailed comparison of density, power, and performance for different circuits between Crosstalk and CMOS technology. For comparison, both Crosstalk and CMOS circuits are simulated using ASAP7 PDK and keeping nominal VDD at 0.7V. The benefits are significant in all aspects of Crosstalk logic based implementations. In terms of transistor count, the highest reduction was for the mux circuit, it was 62%. For cm85a and pcle circuits the reduction in transistor count are 59% and 23% respectively. Crosstalk circuits show on average 58% power benefits over CMOS counterparts. The benefits are primarily due to the reduction in transistor count. For primitive cells, transistor count reduction is 25% for both NAND and NOR gates. However, the reduction in average power for the mux circuit is not much even though transistor count reduction is maximum compared to other circuits. This is because mux circuit implementation requires many pass-gate type circuit styles which results in more switching activities, hence, less power reduction. The effect can also be seen for performance (Table I) where CMOS technology shows better performance than Crosstalk. However, for cm85a and pcle circuits, Crosstalk circuits have 10% and 53% improvement in performance respectively.

VI. CONCLUSION

In this paper, we presented Crosstalk computing's scalability aspects. Using ASAP7nm PDK, we have shown that for both best case and worst case process variations, Crosstalk circuits can be designed to function properly, and benefits over CMOS can be achieved. We have also shown implementation of three MCNC benchmark circuits and compared density, power and performance results with respect to CMOS at 7nm. Our results show significant benefits over CMOS; for the best case, there is 62%, 30% and 53% reduction in density, power, and performance, respectively.

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