From 180nm to 7nm: Crosstalk Computing Scalability Study

Md Arif Iqbal[1], Naveen Kumar Macha, Bhavana Tejaswini Repalle, Mostafizur Rahman[2]
Computer Science & Electrical Engineering, University of Missouri Kansas City, Kansas City, Missouri
mibn8@mail.umkc.edu[1], rahmanmo@umkc.edu[2]

***Abstract*— Crosstalk computing is a novel computing technology that relies on interference between adjacent interconnects to achieve logic function. By engineering coupling capacitance in an innovative circuit scheme, all primitive cells and custom logic can be implemented with significant gain. In this paper, we report on the scalability aspects of this technology and show for primitive circuits how the circuit properties evolve from one node to other. We also present comparison results for several benchmarking circuits. Some significant results are: for primitive NAND gate, designed in 180nm, 65nm, 32nm, and 7nm technology nodes, the average reduction in power is 42.5% and an average reduction in performance is 34.5% comparing to CMOS for all mentioned nodes. For benchmarking circuits designed at 7nm, there are 48%, 57%, and 10% improvements against CMOS designs in terms of density, power, and performance respectively.**

I. Introduction

Crosstalk computing provides a new mindset for computing by leveraging interconnects. In this technology, nanoscale metal lines are arranged in a manner such that the interference between them can be tuned to obtain logic [1]-[5]. Fig. 1(i) shows an abstract view of the fabric, where CMOS control transistors are at the bottom and logic specific metal arrangements are on top. The dielectric between the metal lines will dictate the capacitance between them and can be tuned for desired logic. Respective schematic view of NAND and NOR are given in Fig.1(ii). During logic computation, the victim net (*Vi*) voltage is controlled electrostatically through coupling capacitances between two aggressors (*Ag1* and *Ag2*) and victim (*Vi*) net. To drive the *Vi* node for the next round of logic evaluation, its voltage is discharged to ground through a transistor controlled by *dis* signal after every round of logic evaluation. Thus, the *Vi* node is connected to an inverter acting as a threshold function on one end and connected to the drain side of the discharge transistor on the other end. This principle is used while implementing both NAND and NOR gates with the only difference of coupling strengths (C_{ND} & C_{NR}) between inputs and *Vi* net.

II. Scalability Aspects of Crosstalk Circuits

For any new emerging technology to compete/co-exist with CMOS, scalability study is one of the key requirements. As a part of scalability study, Crosstalk logic gates are designed using 180nm, 65nm TSMC PDK, 32nm PTM model and 7nm ASAP PDK [6]. We have designed primitive gates for both Crosstalk and CMOS in all four nodes and analyzed power, performance under various process variation. In Crosstalk computing, inverter and discharge transistors are technology dependent. Our results indicate that devices with better I_{ON}/I_{OFF} ratio and lower supply voltage contribute in lower power (Fig. 3) and better performance (Fig. 4) for Crosstalk circuits compared to CMOS under process variations. Additionally, our results also suggest that coupling capacitance of Crosstalk circuits reduces with the shrinking of technologies (Fig. 5) because of the lower threshold voltage of the devices in advanced nodes, resulting in less amount of voltage accumulation required in *Vi* node to change the output stage of the inverter. From Fig. 3 it can be seen that both CMOS and Crosstalk NAND & NOR gate show reduction in power; however, Crosstalk gates show ~42.5% more reduction in power than CMOS gates for all the technology nodes. The improvement in power for Crosstalk gates is because of less number of active devices and lower effective load due to the series connection of coupling capacitance to the inverter. Fig. 4 shows the performance results of Crosstalk gates with respect to CMOS for various process corners. For typical process corner, there is an average improvement of 34% in performance for Crosstalk gates compared to CMOS for all technologies. As shown in Figs. 4(i&ii), for slow process corner, the performance is the worst due to slow PMOS and NMOS devices whereas for the FF corner the performance is the best due to the fast active devices. Such performance improvement in Crosstalk circuits is due to lower effective load capacitances, lower interconnect parasitic and shorter VDD/GND to output rail. Moreover, reliance on signal interference for computation and 3-D layout scheme, less number of transistor required for implementing complex function [5] maximizes the density gain for Crosstalk over CMOS counterparts as can be seen from Fig. 2. To demonstrate the benefits of Crosstalk circuits for larger logics and to show the implementation in advanced nodes, we have designed three large MCNC benchmark circuits (cm85a, mux, and pcle) at 7nm with Crosstalk primitive gates and compared the results with CMOS (Table I). Highest density benefit can be seen for mux circuit, 62% reduction in transistor count which also translates in a reduction in power by 59%. However, due to the cascaded nature and circuit layout, performance improvement is less compared to other circuits.

III. Conclusion

In this paper, we have shown that Crosstalk circuits can be designed at different technology nodes. Our results show significant improvement in density, power, and performance for Crosstalk circuits compared to CMOS even with scaling down of technology nodes.

References

[1] N. K. Macha *et al.*, 2017 ICRC. [2] N. K. Macha *et al.*, 2018 NANOARCH, [3] N. K. Macha *et al.*, 2018 ICRC. [4] N. K. Macha *et al.*, 2019 Aerospace Conference.[5] A. Iqbal, *et al.*, https://arxiv.org/abs/1904.03294.[6] L. T. Clark, 2016 Microelectronics Journal, vol. 63, pp. 105-115.

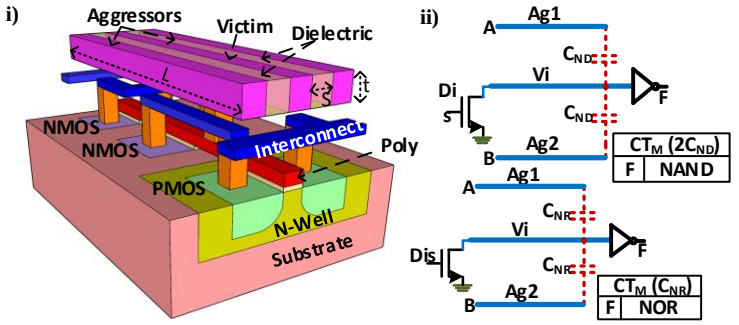

Fig. 1.i) Abstract view of Crosstalk computing Fabric; coupling capacitances will be on the top denoted as 'dielectric' in between nano-metal lines denoted as 'aggressors' and 'victim'. ii) Schematic of primitive cells (NAND & NOR) in Crosstalk fabric. Inputs will be given through metal lines and coupled with *Vi* line for logic computation.

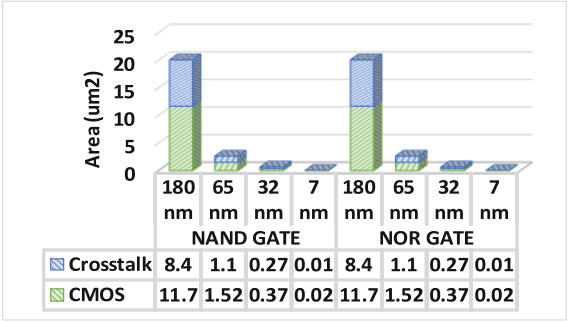

Fig. 2. Impact on area of Crosstalk logic gates due to scaling of technology nodes. Logic gates are designed in 180nm, 65nm, 32nm, and 7nm nodes. Area required for Crosstalk fabric is less than CMOS due to 3-D circuit style and less active devices.

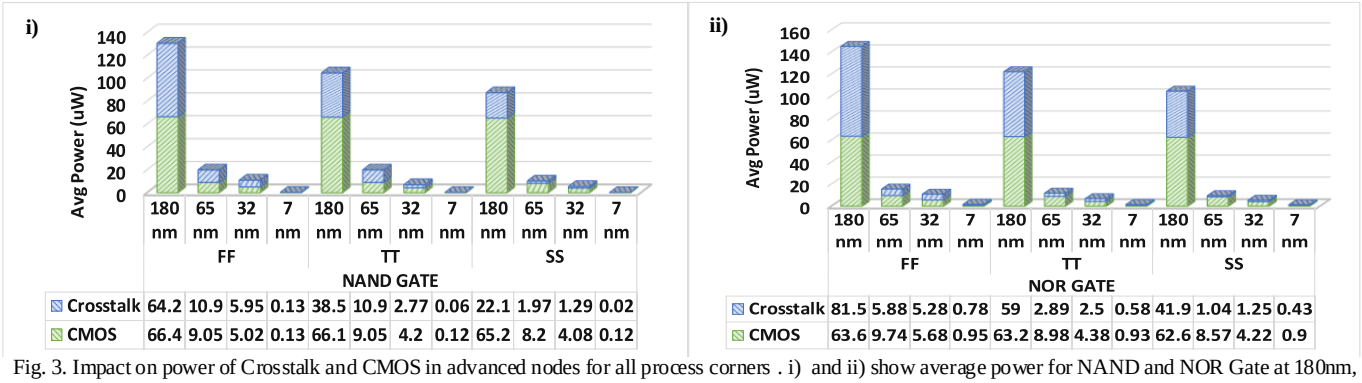

Fig. 3. Impact on power of Crosstalk and CMOS in advanced nodes for all process corners . i) and ii) show average power for NAND and NOR Gate at 180nm, 65nm 32nm and 7nm with process variations. As technology scales down power consumption also reduces for both Crosstalk and CMOS, however Crosstalk computing shows more improvement in power than CMOS; average reduction in power is 42.5% for all technology nodes.

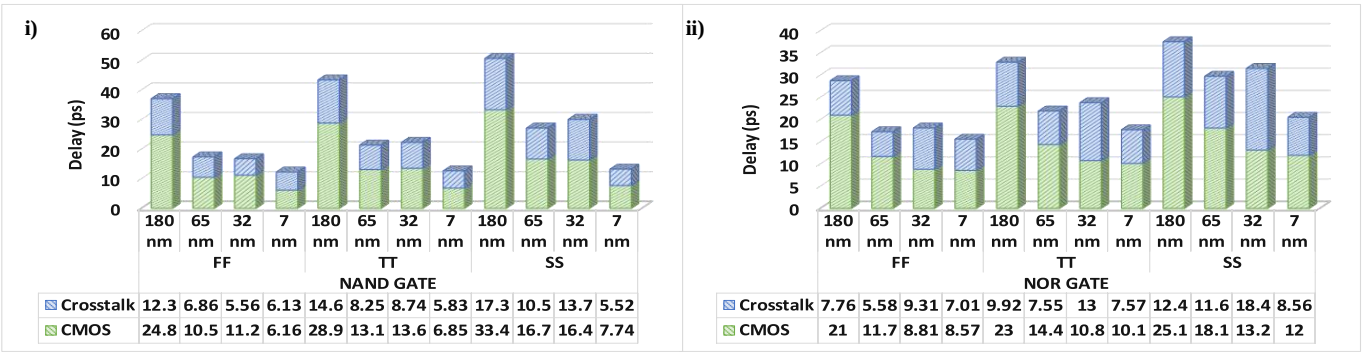

Fig. 4. Technology scaling impact on the performance for Crosstalk and CMOS primitive gates with process variation i) and ii) shows the performance for NAND and NOR Gate. Both of the gates are designed in 180nm, 65nm 32nm and 7nm with process corners. Crosstalk gates have better performance than CMOS logic gates; average improvement in performance for Crosstalk logic gates is reported as 34.5%

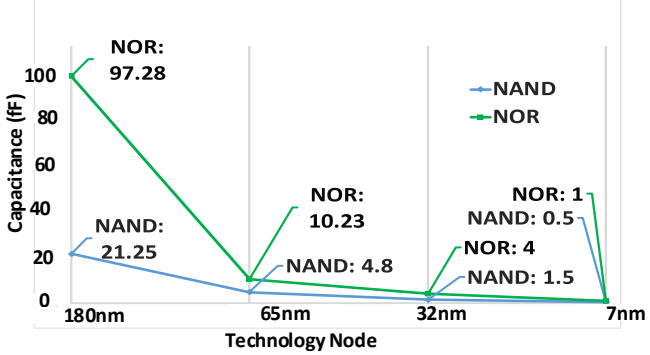

Fig. 5 Change of Coupling Capacitance in advanced technology nodes. Coupling capacitance is calculated for both NAND and NOR gate for 180nm, 65nm, 32nm and 7nm technology. At lower nodes, coupling capacitance reduces significantly ranging from 500aF to few fFs

Table I. Comparison of MCNC Circuits between Crosstalk and CMOS circuits at 7nm to show the implementation of Crosstalk circuits in advance node

MCNC Circuit	Transistor Count			Average Power (uW)			Performance (ps)		
	CMOS	*CT*	*%R*	*CMOS*	*CT*	*%R*	*CMOS*	*CT*	*%R*
Cm85a	168	69	59	60.63	29	52.3	21.1	18.9	10.3
Mux	506	190	62.5	73.7	29.9	59.4	9.43	12.8	-35.2
Pcle	328	252	23.2	288	110	61.8	15.04	7.07	53