Interconnect Crosstalk based Computing for Analog Electronics

Bhavana Tejaswini Repalle, Rajanikanth Desh, Naveen Kumar Macha, Sehtab Hossain, Mostafizur Rahman
Department of Computer Science & Electrical Engineering, University of Missouri Kansas City, MO, USA
E-mail: { brkf9, rd2n8, nmhw9, shgf4}@mail.umkc.edu, rahmanmo@umkc.edu}

Abstract— Analog CMOS faces difficulties in scaling due to the strict requirements of gain, transresistance, transconductance etc., from Analog components, which is achieved through precise customization of transistors. Novel approaches to achieve the core analog components like comparator, Digital to Analog Converter (DAC), Analog to Digital Converter (ADC) etc. with benefits in chip footprint, transistor count and power consumption can open up possibilities for scalable and efficient analog circuits. We propose a novel direction where deterministic interference between Nano-metal lines is leveraged for analog computing. In this approach, the metal lines are coupled and interact through aggressor-victim scenario. Aggressor nets are coupled to victim nets through virtual lateral capacitance. When the input transitions on the aggressor nets, a resultant summation charges are introduced onto the victim nets. If the transitions are opposite, their effects get cancelled. These principles are utilized to achieve summation, subtraction and comparison operations. For DAC, each bit in the digital code are passed through aggressors that couple to a single victim net. By tuning the coupling strength between aggressors and victim in ascending order from LSB to MSB, proportionate analog output is achieved. For ADC, a novel tree-like circuit paradigm is used to distribute sampled analog input signal to the leaf nodes and a branch switching circuitry gives the final digital code. All Crosstalk analog components are implemented at 16nm node and show huge saving in number of devices and power consumption.

Keywords—Comparator, Analog to Digital Converter, Digital to Analog Converter, Aggressor net, Victim net, Crosstalk Analog Components

I. INTRODUCTION

The input and output interface for the digital electronics is always analog. Analog electronics using CMOS technology are hard to scale down and their area is more when compared to digital components on a chip. So, to reduce the area of the analog blocks is to find the portions of it where we can design them by using our novel crosstalk computation technique. In this paper we proposed the preliminary designs for analog blocks using novel crosstalk computation method [1]. We proposed crosstalk computing-based circuits for comparator, DAC, ADC which are the essential analog components. Section II describes the basic principle of crosstalk computation and its basic phenomena. Section III describes about the architecture of analog components – DAC, ADC and Comparator using the novel crosstalk computing technique. Section IV shows the simulation results for the Crosstalk analog designs.

II. CROSSTALK COMPUTATION

In crosstalk phenomena, computation happened through metal lines. The metal lines which we give input voltages are called aggressor nets and the output metal line is called victim nets. In the crosstalk computation mechanism, as shown in the Fig.2.1, whenever the inputs are transitioning in the aggressor nets, then some voltage gets induced on to the victim net. Here, we engineer the coupling capacitance between the metal lines by using different dielectric material. There are two mechanisms takes place depending on the way we give the inputs to the aggressor nets. They are charge summation and charge subtraction phenomena's as explained below.

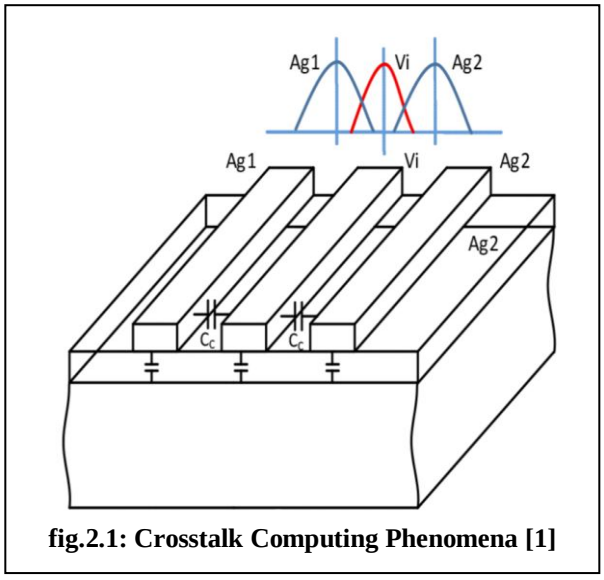

fig.2.1: Crosstalk Computing Phenomena [1]

A. *Charge summation phenomena*

When the inputs transitions on the aggressor nets in the same direction, then the summation of the charges are introduced onto the victim net.

B. *Charge Subtraction phenomena*

If the inputs transitions are in the opposite direction and equal, their effects get cancel. If the input transitions are not equal but opposite, their difference get induced onto the victim net.

III. Analog Components Using Crosstalk

Using the above two basic crosstalk phenomena's we implemented DAC, ADC and comparator.

A. *Crosstalk DAC*

In Crosstalk DAC design which is shown in fig.3.1, each bit in the digital input is given to aggressor nets which are coupled to the victim net with different coupling strengths. The coupling strengths to these aggressor nets are given in ascending order from LSB to MSB. This corresponds to each digital code combination on aggressor nets resulting to a proportionate discrete level on the victim net which can be further processed to a continuous analog signal using reconstruction filter and amplifier. D3, D2, D1, D0 are the input digital code which are given to aggressor nets. Output is taken from the transmission gate which is connected to the victim net (Vi). We are using the discharge transistor to control the floating victim net. Whenever the input bits are transitioning, their induced charges are gets added onto the victim net.

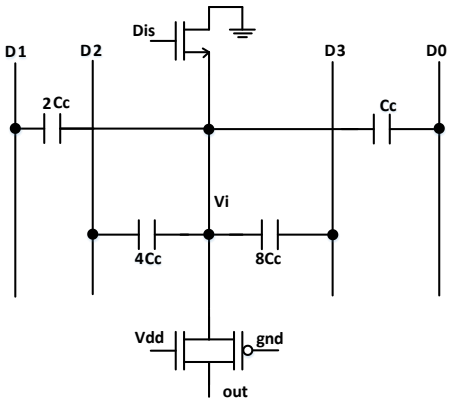

Fig.3.1: Crosstalk 4-bit DAC design

If we use the crosstalk DAC in high frequency range, we can directly pass the staircase output analog signal through reconstruction filter to get the smooth analog signal.

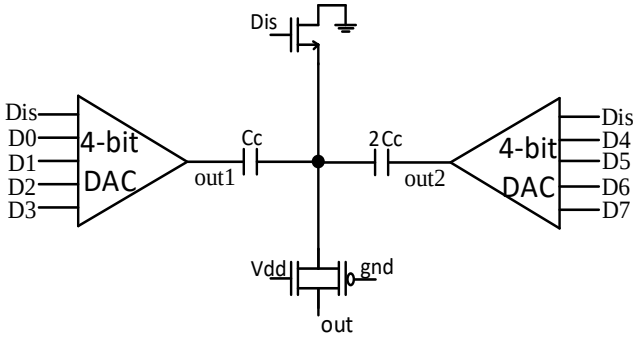

Fig.3.2: 8-bit CT DAC using two 4-bit DAC's

But for low frequency signals, due to long time discharging, reconstruction filter may not produce the unambiguous analog signal. So, to avoid that problem we can design other crosstalk DAC (DAC2) with Dis' signal giving to the discharge transistor. When Dis=0, then we select the DAC1 output and when Dis=1, we select the DAC2 output, the multiplexed staircase output analog signal can be passed through the reconstruction filter. We use low resolution DAC's and by cascading them we can obtain high resolution DAC. For a 5-bit DAC, we can use the 4-bit DAC along with the other aggressor net which is coupled to the victim net with coupling capacitance 16Cc and is driven by the MSB bit (D4). In the similar way, we can design the 8-bit DAC using two 4-bit DAC's as shown in fig.3.2.

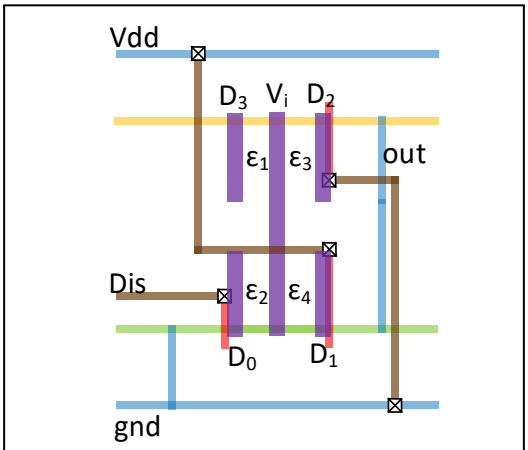

Fig.3.3: Stick Diagram for Crosstalk DAC

Fig.3.3, shows the stick diagram of 4-bit crosstalk DAC, where the four aggressor lines (D0, D1, D2, D3) are capacitively coupled to the victim net (Vi). Their coupling strengths depends upon the different dielectric material between them.

B. *Crosstalk ADC*

For Crosstalk ADC design, we present a novel crosstalk tree-based mechanism which distributes the sampled analog signal to the leaf nodes of the tree in proportion to the coupling strengths of the branches, where a branch switching circuitry gives the final digital code.

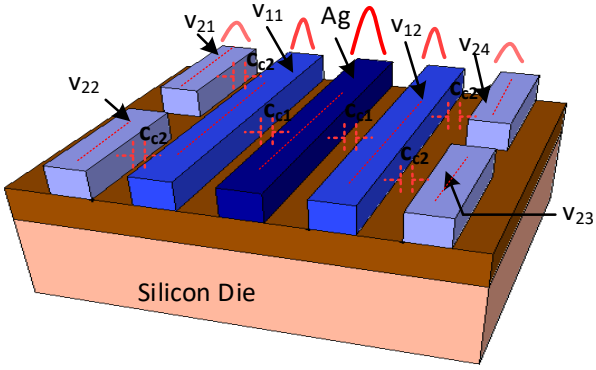

Fig.3.4: Crosstalk ADC design Principle

Fig.3.4, shows the basic principle of crosstalk ADC, where we have one aggressor net which is coupled to two other victim nets with different coupling strengths, then these two victim

nets are coupled to two other child victims nets and it goes on depending on the resolution of the ADC.

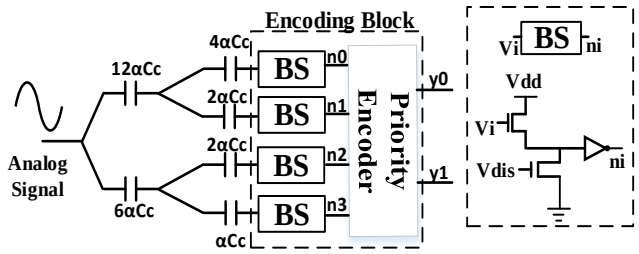

Fig.3.5: 2-bit CT ADC Architecture

Fig.3.5 shows the architecture of 2-bit ADC implemented using the capacitance tree network. There are 4 leaf nodes, means an input signal in the root is divided into 4 segments through coupling; the coupling strength between root and branches varies in descending fashion from top to bottom.

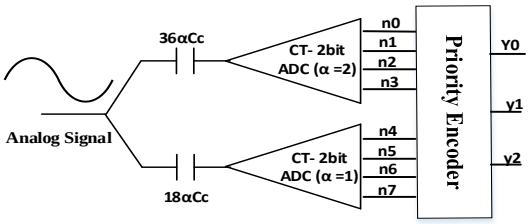

Fig.3.6: 3-bit CT ADC Architecture

At each leaf, there is a branch select (BS) circuit, which consists of a pass transistor to pass 1/0 depending on leaf voltage, an inverter to restore the signal and a discharge transistor to discharge floating voltage and to prepare for next round of conversion. The leaves outputs are called thermometer code which is given to a Priority Encoder-PE for final digital output.

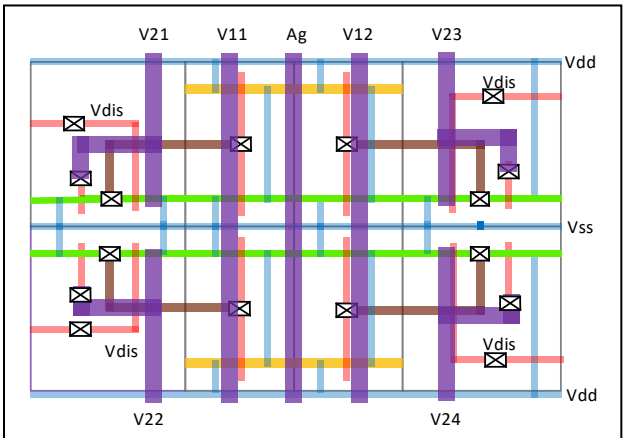

Fig.3.7. Crosstalk 2-bit ADC stick diagram

Similarly, Fig.3.6 shows the schematic of the CT 3-bit ADC, in which two 2-bit ADC networks are connected in parallel to a root aggressor, forming 8 branches. The multipliers α=2 and α=1 are to maintain coupling strengths for 8 branches in descending fashion. These CT ADC circuits are implemented with very less number of transistors, hence IC footprint required is very less, and we have shown this using a stick-diagram layout of 2-bit ADC in Fig.3.7.

C. Crosstalk Comparator

For analog comparison using crosstalk phenomena, the sampled analog input signal (V_{ana}) is given to the first aggressor net and a reference signal (V_r) is given to the second aggressor net as shown in Fig.3.8. The victim net receives sufficient charge to flip the thresholding device like inverter, only when the input signal amplitude is greater than the reference signal amplitude thus, performing comparison.

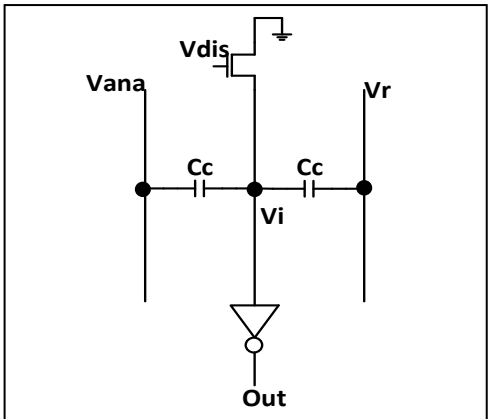

Fig.3.8: CT Comparator Design

The stick diagram for the analog comparator is shown in the Fig.3.9.

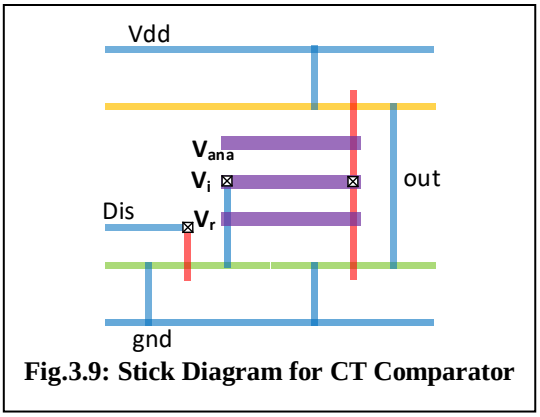

Fig.3.9: Stick Diagram for CT Comparator

IV. RESULTS

A. Crosstalk DAC Simulation Results:

A 4-bit digital signal (D3,D2,D1,D0) is given as input (Fig.4.1) with D3 as MSB and D0 as LSB. From the input signal from 0000 levels to 1111 level, the analog sampled

voltage level increases as shown in the panel4. To increase the output signal strength, we pass this signal through amplifier.

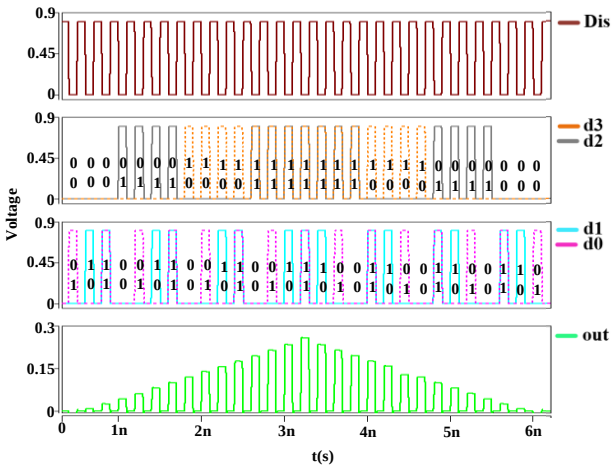

Fig.4.1: Crosstalk DAC Simulation Result

B. Crosstalk ADC Simulation Results:

A sampled sinusoidal analog signal with 4 levels is given as input (Fig.4.2). For L1, leaves n0-n3 responds as 1110, for L2 it is 1100, for L3 it is 1000, and finally for L4 it is 0000. This response follows the thermometer code which is given to a Priority Encoder-PE. The output from PE is shown in panel-4, which is, 00, 01, 10 and 11 for L1, L2, L3 and L4 discrete levels respectively.

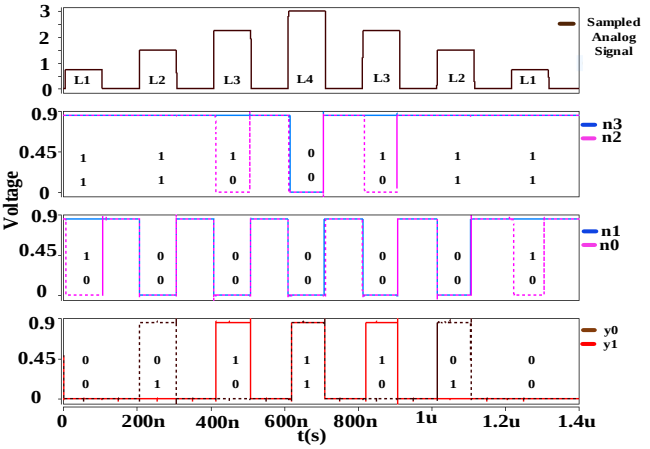

Fig.4.2: 2-Bit Crosstalk ADC simulation result

In Fig.4.3, panel-1 shows 8 sample and hold levels, panel 2-4 show the outputs of 8 BS blocks, and panel4 shows the PE output. For L1-L8, BSs responses are 11111110-00000000, and PE responses are 000-111.

C. Crosstalk Comparator Simulation Results:

As shown in the Fig.4.4, the analog signal applied to the comparator is a staircase signal varying from 0-3V with the 0.1V difference. In the waveform, the ref signal is a 1.5V signal, whenever the analog signal reaches above 1.5V then the inverter flips the output, here we used other inverter to get the non-inverted result.

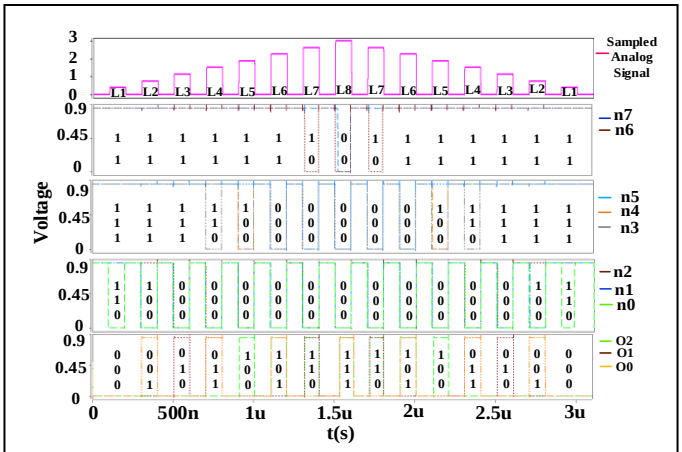

Fig.4.3: 3-Bit Crosstalk ADC simulation result

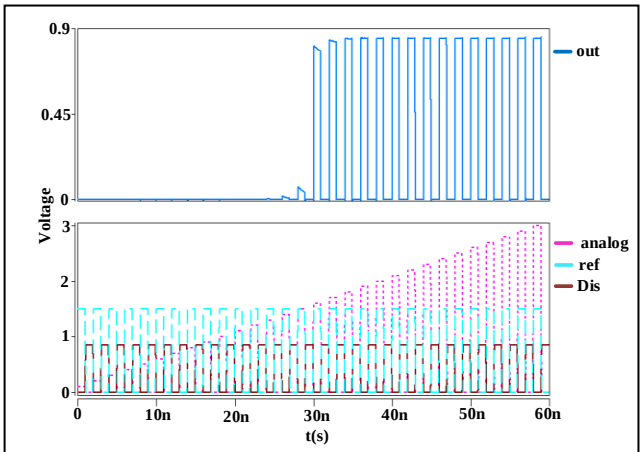

Fig.4.4: CT Comparator Simulation results

D. Properties of our Crosstalk Analog components:

Analog Module	Parameters of the analog components using Crosstalk computing technique		
	Area (nm^2)	*Bandwidth*	*No.of transistors required*
4-bit DAC	12,480	10MHz-10GHz	3
2-bit ADC(without PE)	22,176	1kHz-100MHz	16
Comparator	12,288	1GHz-50GHz	3

V. CONCLUSION

In this paper, we introduced the preliminary explorations of the Crosstalk analog components – DAC, ADC and comparator using crosstalk computation method, these designs uses a less number of transistors compared to the present analog designs where we can see the more area reduction. Our future work is to improve performance and to increase resolution of DAC and ADC.

VI. References

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