Mostafizur Rahman

University of Missouri-Kansas City
570A Flarsheim Hall, 5100 Rockhill Rd
Kansas City, MO 64110

Phone: (816)-235-5939
Email: rahmanmo@umkc.edu;
m.rahman@computing-lab.com
Group website: http://computing-lab.com

Title Assistant Professor

Department Computer Science & Electrical Engineering, University of Missouri Kansas City

Education

University of Massachusetts Amherst	Electrical & Computer Engineering	PhD	Spring, 2015
North South University, Bangladesh	Computer Engineering	BSc	Spring, 2008

Current and Previous Academic Positions

University of Missouri-Kansas City	Assistant Professor	06/ 2015- Present
University of Massachusetts Amherst	Research Assistant	05/2010-05/ 2015
University of Massachusetts Amherst	Graduate Teaching Assistant	09/2014-05/2015
North South University	Undergraduate Teaching Assistant	05/2007-12/2007

Other Professional Experience

Intel Corporation	Component Research Trainee	05/ 2013- 08/2013

Research Area

Machine intelligence, hardware security assessment and prevention in ASIC and Reconfigurable computing architectures, hardware-software co-integration for robotics and machine learning acceleration, non Von-Neumann computing with emerging technologies and architectures, modeling and simulation across system layers from device to circuits, and experimental prototyping.

Grants

Agency: ***National Science Foundation***
Title: II-NEW: Experimental Characterization and CAD Development Testbed for Nanoscale Integrated Circuits
Amount: $772,061.00, Duration: 2016-2019
Role: Co-PI (share $257.3K)

Agency: ***National Science Foundation***
Title: ICorps: Seeking Commercialization Potential of a New Computing Paradigm with Interconnect Crosstalk for Future Electronics
Amount: $50,000.00, Duration: 2019
Role: PI

Agency: ***University of Missouri Kansas City***
Title: Prototyping Crosstalk Computing Chip for Future Electronics
Amount: $18,000.00, Duration: 2018-2019
Role: PI

Agency: ***Office of Naval Research***
Title: FPGA Vulnerability Analysis Tools, Phase I
Amount: $250,000.00, Duration: 2019-2020
Role: Subcontract PI (Share $72K)

Agency: ***Honeywell***
Title: Senior Design Projects
Amount: $10,000.00, Duration: 2019-2020
Role: PI

Agency: ***NSF PFI (pending result)***
Title: Crosstalk Computing for Future Secured Electronics
Amount: $250000.00, Duration: 2020-2022
Role: PI

Agency: ***NSF SBIR (pending result)***
Title: Messaging based Intelligent Computing for AI Inference
Amount: $256,000.00, Duration: 2020-2021
Role: Lead (Crosstalk LLC), UMKC Subcontract

Agency: ***Federal Appropriation Grant (pending result)***
Title: Pathfinding for Next-Gen Trusted Microelectronics
Amount: $8,000,000.00, Duration: 2021-2026
Role: Co-PI

Honors and Awards

- Best Paper Award, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), Paris, France, 2014.
- Best Paper Award, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), New York, USA, 2013.
- 2nd Prize, University of Massachusetts Innovation Challenge, 2011
- Co-Authored 2 Best Research Poster Awards: 2011, 2012 at FCRP-DARPA FENA Center Annual Sponsor Reviews, at MIT and UCLA

In the News

- "New Center for Nanotechnology" SCE News Cover Story, https://sce.umkc.edu/2016/09/02/new-center-nanotechnology/
- "4 Strange New Ways to Make a Computer" IEEE Spectrum Feature Story 2018 https://spectrum.ieee.org/nanoclast/computing/hardware/4-strange-new-ways-to-make-a-computer
- Featured article in Advances in Engineering online magazine https://advanceseng.com/possible-solution-next-generation-3-d-ics-thermal-challenge/

Invited Talks

- "Stacked Horizontal Nanowire based 3-D IC for Future High-Performance Computing", Beyond CMOS Workshop: Interconnect Challenge, 2017, Oak Ridge National Laboratory & Department of Energy
- "Vertical Nanowire based 3-D Integrated Circuits for Beyond CMOS" CSEE Departmental Seminar, University of Missouri Kansas City, 2017
- "Nanotechnology for Future Computing Needs", IEEE Electronics Local Chapter Meeting, 2016

Student Awards

- UMKC Financial Aid & Scholarship, Joshua Banago, 2019
- HCA Scholarship for Undergraduate Studies, Joshua Banago, 2019
- Ronald A. MacQuarrie Graduate Fellowship, Naveen Kumar Macha, 2019
- School of Graduate Studies Research Fellowship award, Naveen Kumar Macha, 2018, 2019
- School of Graduate Studies Research Fellowship award, Arif Iqbal, 2017
- SGS Travel grant to attend IEEE/ACM International Symposium on Nanoscale Architectures, Naveen Kumar Macha, 2017
- SGS Travel grant to attend IEEE/ACM Rebooting Computing Conference, Naveen Kumar Macha, 2018
- SGS Travel grant to attend IEEE/ACM Rebooting Computing Conference, Bhavana Tejaswini Repalle, 2018
- NSF student Travel grant to attend HOST conference, Naveen Kumar Macha, 2018

Patents

- Darrel Schlom, Mostafizur Rahman, Kelin Kuhn, John Heron, "Low-energy Consumption Quaternary Magnetoelectric Spin Hall Effect Based Logic and Memory Device", WO2017214628A1, 2017
- Mostafizur Rahman, "Messaging based Intelligent Processing Unit", 2020 (Provisional Patent Filed)
- Mostafizur Rahman, Naveen Kumar Macha, "CROSS-TALK COMPUTING FOUNDATION for DIGITAL LOGIC", 2019, US20190356315A1

Certifications

- UMKC Faculty Certification in Online Teaching and Learning, 2020
- ACUE Effective Online Teaching Practices for Higher Ed (2020-2021: Currently ongoing)

Membership in Professional Society

Member, IEEE (Institute of Electrical and Electronics Engineers)

University Committee Assignments

- Coordinator, Higher Learning Commission Committee for Bachelor of Computer Science & Electrical Engineering (May 2017- present)
- Member, Undergraduate Degree Program Committee (Sep. 2015- present)
- Member, PhD Degree Committee- ECE Focus (Sep. 2015- present)

Editorship & Services to Professional Society

- Publication Chair, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH) 2017, New Port, RI, USA
- Guest Editor, Special Issue on 3-D Integrated Circuits in IEEE Transactions on Nanotechnology (July. 2015- 2018)
- Publication Chair, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH) 2015, Boston, USA
- Session Chair, "Nano MEMS", IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH) 2015, Boston, USA
- Session Chair, "All Spin Logic", IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH) 2016, Beijing, China
- Best Paper Select Committee Member, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH) 2016, Beijing, China
- Program Committee Member, IEEE VLSI Design Conference 2016-2019, Calcutta, India

Courses Taught

- Nanoscale Devices and Circuits (ECE 5590), Fall 2015, 2016, 2017
- Nanoscale Manufacturing and Integration (ECE 5590), Spring 2016, 2017
- Computer Design and Organization (ECE 424), Fall & Spring 2017, 2018
- Logic Design (ECE 226), 2018, 2019
- Introduction to Computer Organization (ECE 228), Spring 2018, 2019, 2020
- Senior Design I & II (ECE 402, ECE 403), Fall 2019, Spring 2020
- Undergraduate Research (Comp Sci 499), 2015, 2016, 2017, 2018, 2019
- Graduate Research (ECE 5599), 2015, 2016, 2017, 2018, 2019
- Directed Reading (ECE 5597), 2015, 2016, 2017, 2018, 2019
- VLSI Lab (ECE 401VL), Spring 2018

Publications

Google Scholar Citations – 205

https://scholar.google.com/citations?user=hiPxuQQAAAAJ&hl=en

Book Chapter

Santosh Khasanvis, Mostafizur Rahman, Prasad Shabadi, Csaba Andras Moritz, "Unconventional Nanocomputing with Physical Wave Interference Functions", in Nanomagnetic and Spintronic Devices for Energy-Efficient Memory and Computing, J. Atulasimha and S. Bandyopadhyay, Eds., Wiley , pp. 291-328, 2015

Journals

1. Wafi Danesh, Joshua Banago, Mostafizur Rahman, "Turning the Table: Using Reverse Engineering Techniques to Detect FPGA Trojans", *Journal of Hardware and Systems Security*, Springer, 2020 (Under Review)
2. Sehtab Hossain, Md Arif Iqbal, Mostafizur Rahman, "More than a Device: Function Implementation in a Multi-Gate Junctionless FET Structure", *IEEE Transactions on Circuits and Systems I*, 2020 (To be submitted)

3. Naveen Kumar Macha, Md Arif Iqbal, Bhavana Tejaswini Repalle, Sehtab Hossain, Mostafizur Rahman, “Crosstalk Noise based Configurable Computing: A New Paradigm for Digital Electronics”, *Nature Electronics* (Under Review), 2020
4. Naveen Kumar Macha, Bhavana T Repalle, Arif Iqbal, Mostafizur Rahman, On the Signal Integrity for Large Scale Design While Computing with Noise, *IEEE Transactions on Nanotechnology*, 2020 (To be submitted)
5. Naveen Kumar Macha, Bhavana T Repalle, Mostafizur Rahman, Fine-Grained Polymorphic Circuit Framework in Crosstalk Computing, ACM Journal on Emerging Technologies. 2020 (Under Review)
6. Arif Iqbal, Naveen Kumar Macha, Mostafizur Rahman, Thermal Management Challenges and Mitigation Techniques for Transistor-level 3-D Integration, *Elsevier Microelectronics Journal*,2019
7. N. K. Macha, M. A. Iqbal and M. Rahman, "New 3-D CMOS Fabric with Stacked Horizontal Nanowires," *IEEE Transactions on Computer Aided Design*, Special Issue on 3-D ICs. 2018
8. Jiajun Shi, Mingyu Li, Mostafizur Rahman, Santosh Khasanvis, C. Andras Moritz, “NP-Dynamic Skybridge: A Fine-grained 3D IC Technology with NP-Dynamic Logic", *Transactions on Emerging Topics in Computing*, pp 286-299, March 2017
9. Mingyu Li, Jiajun Shi, Mostafizur Rahman, Santosh Khasanvis, C. Andras Moritz, “Skybridge-3D-CMOS: A Fine-Grained 3D CMOS Integrated Circuit Technology", *IEEE Transactions on Nanotechnology*, Special Issue on 3-D ICs, May 2017
10. Santosh Khasanvis, Mingyu Li, Mostafizur Rahman, Mohammad Salehi Fashami, Ayan K. Biswas, Jayasimha Atulasimha, Supriyo Bandyopadhyay, Csaba Andras Moritz, "Self-similar Magneto-electric Nanocircuit Technology for Probabilistic Inference Engines", *IEEE Transactions on Nanotechnology, Special Issue on Cognitive and Natural Computing with Nanotechnology* , Vol. 14 , No. 6 , 980-991 , 2015
11. Mostafizur Rahman, Santosh Khasanvis, JiaJun Shi, Csaba Andras Moritz, "Wave Interference Functions for Neuromorphic Computing", *IEEE Transactions on Nanotechnology* , Vol. 14 , No. 4 , pp. 742-750 , 2015
12. Santosh Khasanvis, Mingyu Li, Mostafizur Rahman, Ayan K. Biswas, Mohammad Salehi Fashami, Jayasimha Atulasimha, Supriyo Bandyopadhyay, Csaba Andras Moritz, "Architecting for Causal Intelligence at Nanoscale", *IEEE Computer, Special Issue on Rebooting Computing* , Vol. 48 , No. 12 , 54-64 , 2015
13. Santosh Khasanvis, Masum K Habib, Mostafizur Rahman, Roger Lake, Csaba Andras Moritz, "Low-Power Heterogeneous Graphene Nanoribbon-CMOS Multistate Volatile Memory Circuit", *ACM Journal on Emerging Technologies in Computing Systems (JETC) , Special Issue on Advances in Design of Ultra-Low Power Circuits and Systems in Emerging Technologies*, Vol. 12 , No. 2 , Article 15 , pp. 15:1-15:18, August , 2015
14. Mostafizur Rahman, Santosh Khasanvis, & C. A. Moritz, “Nanowire Volatile RAM as an Alternative to SRAM”. *ACM Journal on Emerging Computing*, V-12, Issue 3, pp. 30:1-30.13, 2015
15. Mostafizur Rahman, Santosh Khasanvis, Jiajun Shi, Mingyu Li & C. A. Moritz, “SkyBridge: 3-D Integrated Circuit Technology Alternative to CMOS”. Preprint available at- http://arxiv.org/abs/1404.0607
16. S. Khasanvis, M. Rahman, and C. A. Moritz, “Heterogeneous Graphene-CMOS Ternary Content Addressable Memory”, *Elsevier Journal of Parallel and Distributed Computing*, 71-82, 2013.

17. J. Zhang, M. Rahman, P. Narayanan, S. Khasanvis, and C. A. Moritz, "Parameter Variation Sensing and Estimation in Nanoscale Fabrics", *Elsevier Journal of Parallel and Distributed Computing*, 2013.

Peer Reviewed Conference Papers

1. Wafi Danesh, Joshua Banago, Mostafizur Rahman, "Fast detection of Trojans in FPGA Bitstream", *Computing Frontiers Conference*,2020 (To be submitted)
2. Sehtab Hossain, Md Arif Iqbal, Mostafizur Rahman, A New Approach towards Embedded Logic in a Single Device, *IEEE Nanotechnology Conference* 2020, Montreal, Canada
3. Arif Iqbal, Naveen Kumar Macha, Bhabhana T Repalle, Mostafizur Rahman, Design and Comparison of Crosstalk Circuits at 7nm, *IEEE Rebooting Computing Conference*,2019
4. Arif Iqbal, Naveen Kumar Macha, Bhabhana T Repalle, Mostafizur Rahman, From 180nm to 7nm: Crosstalk Computing Scalability Study, *IEEE Electron Device Society S3S Conference*,2019
5. Arif Iqbal, Naveen Kumar Macha, Bhabhana T Repalle, Mostafizur Rahman, A Logic Simplification Approach for Very Large Scale Crosstalk Circuit Designs, *IEEE/ACM Symposium on Nanoscale Architectures*,2019
6. Naveen Kumar Macha, Bhabhana T Repalle, Arif Iqbal, Mostafizur Rahman, A New Paradigm for Computing for Digital Electronics under Extreme Environments, *IEEE Aerospace Conference*, 2019
7. Naveen Kumar Macha, Bhavana Tejaswini Repalle, Sandeep Geedipally, Rafel Rios, Mostafizur Rahman, A New Paradigm for Fault-Tolerant Computing with Interconnect Crosstalks, *IEEE Conference on Rebooting Computing*,2018
8. Naveen Kumar Macha, Sandeep Geedipally, Bhavana Repalle, Md Arif Iqbal, Wafi Danesh, Mostafizur Rahman, Crosstalk based Fine-Grained Reconfiguration Techniques for Polymorphic Circuits, *2018 IEEE/ACM International Symposium on Nanoscale Architectures*,2018
9. Rajanikanth Desh, Naveen Kumar Macha, Sehtab Hossain, Repalle Bhavana Tejaswini, Mostafizur Rahman, A Novel Analog to Digital Conversion Concept with Crosstalk Computing, *2018 IEEE/ACM International Symposium on Nanoscale Architectures*,2018
10. Naveen Kumar Macha, Sandeep Reddy Geedipally and Mostafizur Rahman, "Ultra High Density 3D SRAM Cell Design in Stacked Horizontal Nanowire (SN3D) Fabric", *IEEE/ACM International Symposium on Nanoscale Architectures*. 2017.
11. Wafi Danesh and Mostafizur Rahman, "Linear Regression based Multi-State Logic Decomposition Approach for Efficient Hardware Implementation", *IEEE/ACM International Symposium on Nanoscale Architectures*. 2017.
12. Wafi Danesh and Mostafizur Rahman, "A New Approach for Multi-Valued Computing Using Machine Learning", *IEEE Conference on Rebooting Computing*. 2017
13. Naveen Kumar Macha, Rakesh Kumar Reddy Vijjapuram, Vinay Chitturi, Sehtab Hossain and Mostafizur Rahman, "A New Concept for Computing using Interconnect Crosstalks", *IEEE Conference on Rebooting Computing*. 2017

14. Arif Iqbal and Mostafizur Rahman, “New Thermal Management Approach for Transistor-level 3-D Integration”, *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference*. 2017
15. Naveen Kumar Macha and Mostafizur Rahman, “Cost Projections and Benefits for Transistor-Level 3-D Integration with Stacked Nanowires”, *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference*. 2017
16. M. Li, S. Khasanvis, J. Shi, S. Bhat, M. Rahman and C. A. Moritz, "Towards automatic thermal network extraction in 3D ICs," *2016 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Beijing, 2016, pp. 25-30.
17. J. Shi, M. Li, S. Khasanvis, M. Rahman and C. A. Moritz, "Routability in 3D IC design: Monolithic 3D vs. Skybridge 3D CMOS," *2016 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Beijing, 2016, pp. 145-150.
18. N. K. Macha, M. A. Iqbal and M. Rahman, "Fine-grained 3-D CMOS concept using stacked horizontal nanowire," *2016 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, Beijing, 2016, pp. 151-152.
19. JiaJun Shi, Mingyu Li, Mostafizur Rahman, Santosh Khasanvis, Csaba Andras Moritz, "Architecting NP-Dynamic Skybridge", in Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch) , pp. 169-174 , 2015
20. Santosh Khasanvis, Mingyu Li, Mostafizur Rahman, Mohammad Salehi Fashami, Ayan K. Biswas, Jayasimha Atulasimha, Supriyo Bandyopadhyay, Csaba Andras Moritz, "Physically Equivalent Magneto-Electric Nanoarchitecture for Probabilistic Reasoning", in Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch) , pp. 25-26 , 2015
21. Mostafizur Rahman, Santosh Khasanvis, JiaJun Shi, Mingyu Li, Csaba Andras Moritz, "Architecting 3-D Integrated Circuit Fabric with Intrinsic Thermal Management Features", in Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch) , pp. 157-162 , 2015
22. Mostafizur Rahman, JiaJun Shi, Mingyu Li, Santosh Khasanvis, Csaba Andras Moritz, "Manufacturing Pathway and Experimental Demonstration for Nanoscale Fine-Grained 3-D Integrated Circuit Fabric", in Proceedings of IEEE International Conference on Nanotechnology (IEEE NANO) , pp. 1214-1217, 2015
23. Santosh Khasanvis, Mostafizur Rahman, Mingyu Li, JiaJun Shi, Csaba Andras Moritz, "Architecting Connectivity for Fine-grained 3-D Vertically Integrated Circuits", in Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch) , pp. 175-180 , 2015
24. Mostafizur Rahman ; Santosh Khasanvis ; Jiajun Shi ; Mingyu Li ; Csaba Andras Moritz, “Fine-grained 3-D integrated circuit fabric using vertical nanowires”, 3D Systems Integration Conference (3-D IC), Page(s):TS9.3.1- TS9.3.7, 2015
25. S. Khasanvis, M. Rahman, & C. A. Moritz, “Spin Wave Fabric for Multi-valued Computations”.IEEE/ACM International Symposium on Nanoscale Architectures (2014) (Best Paper Award)
26. M. Rahman, S. Khasanvis, & C. A. Moritz, “Novel 6T-TRAM Concept for Ultra-Low Power Applications”. IEEE/ACM International Symposium on Nanoscale Architectures (2014)
27. M. Rahman, S.B. Inampudi & S. Kundu, “Functional/Logic Fault Modeling for Addressing the Reliability of MLC NAND Flash Memory”, (In preparation)

28. M. Rahman, P. Narayanan, S. Khasanvis, J. Nicholson, and C. A. Moritz, “Experimental Prototyping of Beyond-CMOS Nanowire Computing Fabrics”, (Best Paper Award), IEEE/ACM International Symposium on Nanoscale Architectures, 134-139 (2013).
29. S. Khasanvis, M. Rahman, P. Shabadi, P. Narayanan, H. S. Yu, C. O. Chui, and C. A. Moritz, “Nanowire Field-Programmable Computing Platform”, IEEE/ACM International Symposium on Nanoscale Architectures, 23-25 (2013).
30. V. Suresh, A. Shanmugam, L. Krishnan, A. Bijjal, M. Rahman, and C. A. Moritz, “Design of 8T-Nanowire RAM Array”, IEEE/ACM International Symposium on Nanoscale Architectures, 152-157 (2013).
31. M. Rahman, P. Narayanan and C. A. Moritz, “Integrated Nanowire Systems for Post-CMOS Computing”, SRC TECHCON. 2012.
32. S. Khasanvis, K. M. M.Habib, M. Rahman, P. Narayanan, R. Lake and C. A. Moritz, ”Ternary Volatile Random Access Memory based on Heterogeneous Graphene-CMOS Fabric”, IEEE/ACM International Symposium on Nanoscale Architectures, 69-76 (2012).
33. M. Rahman, P. Narayanan, and C. A. Moritz,”N3ASIC-based Volatile Nanowire RAM”, IEEE Conference on Nanotechnology, 1097-1101 (2011).
34. P. Narayanan, J. Kina, P. Panchapakeshan, P. Vijayakumar, K. S. Shin, M. Rahman, M. Leuchtenburg, I. Koren, C. O. Chui and C. A. Moritz, “Nanoscale Application Specific Integrated Circuits,” IEEE/ACM International Symposium on Nanoscale Architectures, 99-106 (2011).
35. S. Khasanvis, K. M. M. Habib, M. Rahman, P. Narayanan, R. K. Lake and C. Andras Moritz, ”Hybrid Graphene Nanoribbon-CMOS Tunneling Volatile Memory Fabric”, IEEE/ACM International Symposium on Nanoscale Architectures.189-195 (2011).
36. I. Ercan, M. Rahman, and Neal G. Anderson, ”Determining Fundamental Lower Bounds on Heat Dissipation for Transistor-Based Nanocomputing Paradigms, IEEE/ACM International Symposium on Nanoscale Architectures.169-174 (2011).
37. M. Rahman, ”Comparison of Fast Modular Multiplication in FPGAs”, IEEE International Conference on Anti-counterfeiting, Security, and Identification in Communication, (2010).
38. M. Rahman, I.R. Rokon, Mf. Rahman, ”Efficient Hardware Implementation of RSA Cryptography”, IEEE International Conference on Anti-counterfeiting, Security, And Identification in Communication, (2009).

Recent Presentations (Selected)

- Mostafizur Rahman, “3-D Nanotechnology Fabric for Future Integrated Circuits”, CSEE Departmental Seminar, University of Missouri Kansas City, 2016
- Mostafizur Rahman, “3-D ICs for Beyond CMOS”, IEEE Computer Society Meeting and Dinner with Presentation on the Topic of Nanotechnology Research Advances, Kansas City, 2016
- JiaJun Shi, Mingyu Li, Mostafizur Rahman, Santosh Khasanvis, Csaba Andras Moritz, "Architecting NP-Dynamic Skybridge", IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch) , Boston, USA , 2015
- Santosh Khasanvis, Mingyu Li, Mostafizur Rahman, Mohammad Salehi Fashami, Ayan K. Biswas, Jayasimha Atulasimha, Supriyo Bandyopadhyay, Csaba Andras

Moritz, "Physically Equivalent Magneto-Electric Nanoarchitecture for Probabilistic Reasoning", IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch) , Boston, USA , 2015

- Mostafizur Rahman, Santosh Khasanvis, JiaJun Shi, Mingyu Li, Csaba Andras Moritz, "Architecting 3-D Integrated Circuit Fabric with Intrinsic Thermal Management Features", IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch) , Boston, USA , 2015
- Mostafizur Rahman, JiaJun Shi, Mingyu Li, Santosh Khasanvis, Csaba Andras Moritz, "Manufacturing Pathway and Experimental Demonstration for Nanoscale Fine-Grained 3-D Integrated Circuit Fabric", IEEE International Conference on Nanotechnology (IEEE NANO) , Rome, Italy, 2015
- Santosh Khasanvis, Mostafizur Rahman, Mingyu Li, JiaJun Shi, Csaba Andras Moritz, "Architecting Connectivity for Fine-grained 3-D Vertically Integrated Circuits", IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch) , Boston, USA, 2015
- Mostafizur Rahman, Santosh Khasanvis, Jiajun Shi, Mingyu Li, Csaba Andras Moritz, “Fine-grained 3-D integrated circuit fabric using vertical nanowires”, 3D Systems Integration Conference (3-D IC), Sendai, Japan, 2015

Review Activities

Reviewer for Grant Proposals and Scholarships

- University of Missouri Research Board Funding
- Defense Threat Reduction Agency
- School of Graduate Studies Scholarship

Reviewer for Conferences and Journals

- IEEE Transactions on Nanotechnology
- IEEE Transactions on VLSI Circuits
- IEEE Transactions on Devices
- IEEE Transactions on Multiscale Computing
- ACM Transactions of Emerging Technologies
- IEEE/ACM Conference on Nanoscale Architectures
- IEEE Great Lake VLSI Symposium
- IEEE Conference on VLSI Technologies

Research Supervision

PhD Advising

- Arif Iqbal, Computer Science Electrical Engineering,
  Current status: PhD, estimated completion date: 2020
- Naveen Kumar Macha, Computer Science Electrical Engineering,
  Current status: ASIC Clock Designer (NVIDIA), completion date: 2020
- Wafi Danesh, Computer Science Electrical Engineering,
  Current status: PhD, estimated completion date: 2020

- Sehtab Hossain, Computer Science Electrical Engineering,
  Current status: PhD, estimated completion date: 2020

MS Thesis Advising

- Karthik Reddy, Computer Science Electrical Engineering,
  Current status: Verification Engineer (Qualcomm), completion date: 2016
- Sandeep Reddy Geedipelly, Computer Science Electrical Engineering,
  Current status: Process Engineer (Intel), completion date: 2018
- Bhavana Tejaswini Rapalle, Computer Science Electrical Engineering,
  Current status: Layout Design Engineer (Intel), completion date: 2019

MS Student Advising (Project work)

- Rajanikanth Desh, Computer Science Electrical Engineering,
  Current status: Verification Engineer (Intel), completion date: 2018
- Kaimo Li, Computer Science Electrical Engineering,
  Current status: MS, estimated completion date: 2020

Undergraduate Research *(Sponsored Research)*

- Joshua Banago, Computer Science Electrical Engineering,
  Current status: BS, estimated completion date: 2021
- Richard Hunt, Computer Science Electrical Engineering,
  Current status: BS, estimated completion date: 2021
- Logan McPhillips, Computer Science Electrical Engineering,
  Current status: BS, estimated completion date: 2020

Undergraduate Research *(Research Project)*

- Darius Williams, Computer Science Electrical Engineering,
  Current status: BS, estimated completion date: 2020

Volunteering

- Mentorship at Computer Science Teacher Mentor Day, 2020
- UMKC Summer Camp Workshop in Scanning Electron Microscopy (SEM), July 2019
- High School Student Tour of SEM, September 2019
- Art Institute Student Tour of SEM, September, 2019
- Donnelly College Student Visit of SEM, October 2019
- Partnership with NSBE for DIRE program, 2019 (ongoing)
- Volunteer judge for KC STEM Alliance high school senior design contest, 2016 & 2017
- UMKC SCE promotion committee member, 2016, 2020
- Volunteer Treasurer, Islamic Society of Greater Kansas City