New 3-D CMOS Fabric with Stacked Horizontal Nanowires

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***Abstract*—As 2-D CMOS reaches its fundamental scaling limits due to device, manufacturing and interconnect bottleneck related constraints at the nanoscale, migration to 3-D provides a possible alternative to continue technology scaling in future. Towards that goal, several 3-D integration approaches with multi-die, multi-chip and sequential layers stacking are pursued. However, these approaches only show incremental density benefits and exhibit new challenges such as lack of thermal management, increasing cost and reliability issues. In contrast to these, we proposed a radically different fabric concept, called Stacked horizontal Nanowire based 3-D CMOS (SN3D), on a single die that can offer a paradigm shift in technology scaling as well as design. Using prefabricated and doped stacked horizontal nanowires as fundamental building blocks, the fabric is assembled using architected connectivity and insulation features. Innovations in circuit style for mapping to SN3D's physical framework, and bottom-up material filling based manufacturing techniques are also central to our approach. In this paper, we detail, fabric's core constructs, logic circuits implementation in SN3D fabric, benchmarking methodology and results, and finally the manufacturing aspects. Our circuit analysis reveals tremendous benefits; for a 4-bit full adder design, SN3D shows 11x, 19%, 18% and 6.7x, 8.69%, 9% benefits over state-of-art 2-D CMOS and transistor-level monolithic 3-D (M3D) in terms of density, power, and performance respectively. In addition, our step-by-step TCAD emulation of manufacturing flow establishes feasibility. If realized, the SN3D fabric can be transformative for the semiconductor industry.**

***Index Terms*—Stacked Horizontal Nanowire, 3-D Integrated Circuit, 3-D CMOS, Fine-Grained 3-D, SN3D, 3-D Manufacturing.**

I. INTRODUCTION

As 2-D CMOS scaling options are reaching fundamental limits [1-5], device and circuit integration in the third dimension could yield new pathways for further miniaturization of ICs. Among most promising 3-D IC research directions, layer-layer, die-die and wafer-wafer stacking using Through Silicon Vias (TSVs) [6-9], and sequential 3-D IC [10-12] are actively pursued by industry. However, these approaches only show linear density benefits and suffer from 2-D CMOS's scalability, high cost and thermal management challenges [12]. In addition, since these rely on top-down approaches where silicon layers or dies with circuits are fabricated first and joined later; the sequential joining processes and heterogeneous material quality of layers/dies introduce low yield, reliability and variability issues. In contrast to these, we proposed [13] a novel 3-D IC fabric technology that uses stacked horizontal nanowires [14-16] in a single die for 3-D integration, and overcomes nanoscale challenges.

In our Stacked Horizontal Nanowire based 3-D CMOS approach, called SN3D hereafter, device, circuit, connectivity, heat management and manufacturing aspects are addressed in an integrated manner. In this approach, horizontally stacked suspended nanowires serve as building blocks or templates, and specially architected device, connectivity, insulation, and heat extraction features are formed onto these nanowires through material depositions for fabric assembly. Logic and memory [17] implementation are through CMOS logic and fabric specific physical mapping scheme. High degree of connectivity and heat management in SN3D is achieved by utilizing fabric's intrinsic features. The connectivity and heat management approach in SN3D is in stark contrast to other 3-D CMOS schemes, which are dependent on large-area TSVs and packaging level heat management respectively. In addition, scalability in this fabric is determined by the ability to integrate more circuits vertically, and primarily rely on material deposition techniques that are more controllable in comparison to the extreme lithography dependent device-scaling paradigm of traditional CMOS.

Previously we introduced the SN3D concept in [13]. In this paper, we elaborate on the fabric components, circuit style, and implementations, present benchmarking results, and discuss manufacturing pathways. The key contributions of the paper are-

- Details of fabric constructs including material aspects, dimension and usage, and overall integration for functionality implementation.
- Discussion on SN3D fabric specific circuit mapping scheme with examples such as basic gates and arithmetic circuits.
- Elaboration of benchmarking methodology and comparison results with state-of-the-art 16nm CMOS. The methodology is detailed from device simulation and modeling aspects to circuit design, layout, and architecture.
- Details about SN3D manufacturability. We present the manufacturing pathway and discuss feasibility based on prior work, extensive literature survey and TCAD process emulation.

Our fabric evaluation results indicate huge potentials of SN3D fabric. Our analysis revealed for a 4-bit adder design, SN3D's benefits are 11x, 19%, 18% and 6.7x, 8.69%, 9% over state-of-art 2-D CMOS and transistor-level Monolithic 3-D

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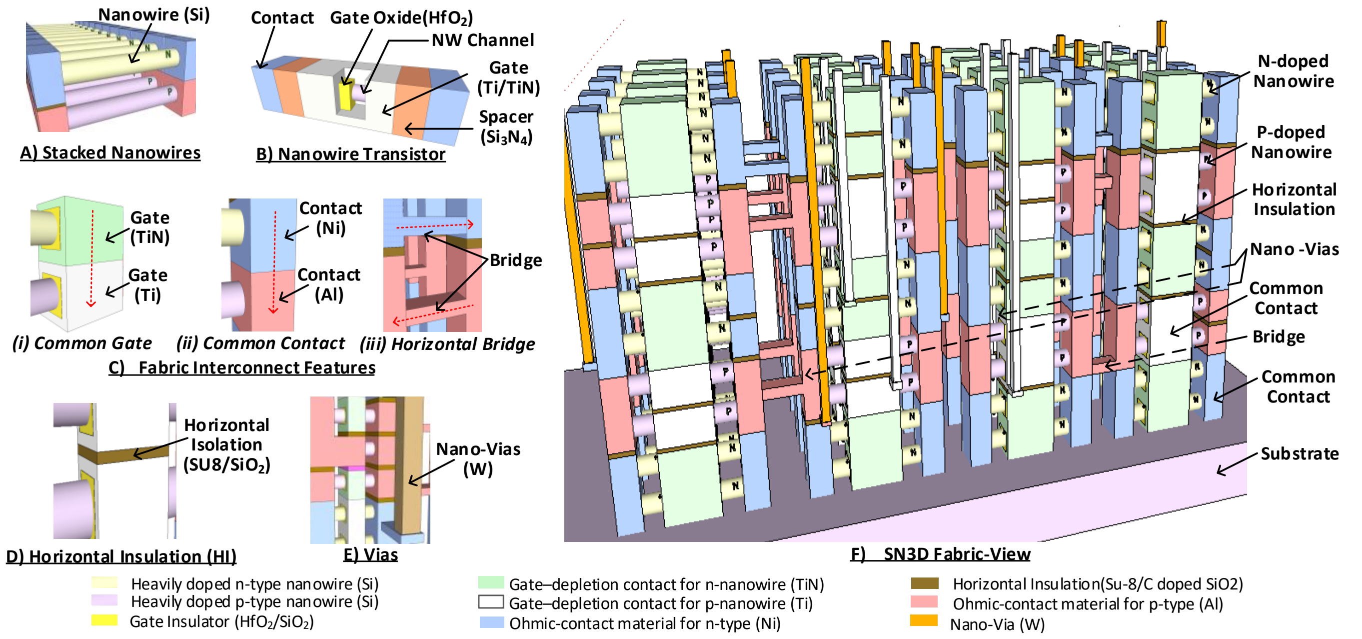

Fig. 1. SN3D fabric and its core components. A) Array of stacked suspended nanowires; B) GAA Junction less transistor; C) Fabric Interconnect: i) Common Gate, ii) Common Contact, iii) Horizontal Bridge; D) Horizontal Insulation; E) Nano-vias; G) Fabric view integrating all components.

(M3D) in terms of density, power, and performance respectively. These advantages are due to high 3-D packing density for devices, very fine-grained 3-D routing, reduced interconnect lengths, and better control of channel in gate all around nanowire transistors. Higher benefits are expected from large-scale circuits due to dense 3-D integration and shorter interconnection requirements [55]. The paper is organized as follows, Section II introduces the SN3D fabric and discusses its core components. Section III shows the CMOS circuit style adopted for SN3D and fabric specific implementation guidelines; elementary circuits and their mapping to SN3D are shown. Section IV details the methodology adopted for fabric evaluation and design rules assumed, TCAD simulation of Junctionless nanowire transistor, and benchmarking results for a range of circuits with respect to 2-D CMOS and transistor level monolithic 3-D CMOS at 16nm, 22nm and 45nm nodes. Finally, we discuss the manufacturing pathway in Section V and draw conclusion in Section VI.

II. SN3D Fabric and Core Constructs

Fig. 1 shows the core components of the fabric and an overview of the circuit mapped SN3D fabric. Stacked suspended horizontal nanowires (Fig. 1A) are the building blocks in SN3D, which are doped and fabricated prior to other steps. Specifically architected fabric components— Nanowire transistors (Fig. 1B), Fabric Interconnects (Fig. 1C), and Horizontal Insulation (Fig. 1D)—are formed onto these nanowires through material deposition techniques [30][33][25][26]. The material choices for SN3D fabric constituents are represented in the figures with different colors and also labeled accordingly. Active devices in this fabric are Gate-All-Around Junctionless nanowire transistors (Fig. 1A) [19] which do not require any doping variation for Drain/Source/Channel regions. In Junctionless devices, the device behavior is modulated by the work-function difference between the gate and heavily doped channel, i.e., under OFF state the nanowire channel (p-type/n-type) is completely depleted, and with a suitable voltage applied (for p-type and n-type) it accumulates the charge to conduct (ON state). Thus, both p and n-type Junctionless transistors can be formed by choosing suitable gate material for p and n doped silicon nanowires respectively [19]. Previously, our group has demonstrated Junctionless device behavior experimentally [25][26]. The 3-D interconnects in SN3D are enabled by using fine-grained fabric interconnects features shown in Fig. 1C. The Common-Gate (CG - Fig.1C.i) feature allows multiple Junctionless devices to be gated with single input in vertical and/or horizontal directions. This enables optimal placement of common gated devices and minimizes inter-device connectivity requirements. The Common-Contact (CC - Fig.1C.ii) feature provides interconnection between adjacent transistors' source and drain contacts (both in vertical and horizontal fashion), thus offer a high degree of freedom in 3D connectivity. Functionally, CG and CC carry common signals, however, physically they are composed of different material stacks according to channel-gate work-function and Ohmic Contact requirements respectively. The Horizontal-Bridge (HB – Fig.1C.iii) serves a dual purpose: connectivity and heat extraction; an HB is placed between an adjacent stack of transistors for interconnection, and for extracting heat from a heated region in 3-D, this is discussed in detail elsewhere [27-29]. The Horizontal-Insulation (HI - Fig.1D) feature provides isolation between adjacent Gate, Source and Drain contacts in the vertical direction. The HBs along with CGs and CCs allow routability in 3-D, and is very different from 2-D CMOS and other TSV based 3-D CMOS approaches where routing mostly take place in the 2-D plane and through vias that connect two layers/dies. Finally, the nano-vias (Fig.1E) are used for input/output signals, and to carry excess routing to top metal layers. Fig.1F shows the SN3D fabric overview, where all the constituent features discussed

above are used to implement large-scale circuits. Intermediate spaces here are filled with a low-K dielectric, which insulates and supports the structures; the dielectric is not shown in figures for transparency of inner structures.

Our proposed SN3D fabric also has intrinsic heat extraction capabilities. Fabric features along with a special heat extraction features aid the heat flow from overheating top transistor and hot-spot regions (distant from heat sink) towards the substrate, thus mitigate the excess temperatures. While fabric's interconnect features (CCs, CGs, and HBs) and nano-vias serve as intrinsic heat extractors, the special heat extraction features composed of thermal junctions and nano-thermal pillars further ameliorate the operating temperatures. These features also give the flexibility to be optimized and placed anywhere in the circuit to extract the heat. Detailed discussion on this is presented in [29][54], where the thermal performance of the SN3D circuit, and different transistor-level 3-D circuits in general, are evaluated based on Finite Element Modeling simulations.

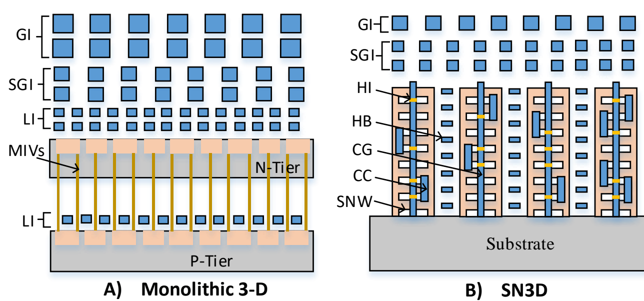

Fig. 2. Conceptual View of Monolithic 3-D and SN3D.

The maximum 3-D benefits achievable in existing 3-D IC approaches is through transistor-level monolithic 3D (M3D) [18], thus we have chosen M3D to benchmark SN3D with respect to. Fig.2 depicts the conceptual view and interconnect hierarchy of M3D IC and SN3D IC. In M3D, thin monolithic inter-vias (MIVs) perforate through the prefabricated-thinned-stacked dies as shown in the Fig.2A, and, interconnect hierarchy of the Local, Semi-Global and Global interconnects remain same as 2-D CMOS. But the die stackability (typically two layers) and MIVs density in M3D are fundamentally limited. Whereas, SN3D is an integrated device-interconnect-fabric as shown in the Fig.2B; active devices are implemented in stacked arrays of nanowires in a dense manner, and 3-D interconnect features (CCs, CGs, and HBs) replace a large portion of metal interconnects. Consequently, the number of semi-global and global interconnects and their wiring lengths on top metal layers (Fig.2B) reduce largely. Thus, in contrast to the other die-stacking and monolithic 3-D approaches, where, only device density is offered, while incremental routing requirement faces the interconnect resource bottleneck, SN3D increases both device density and interconnect resources. Moreover, optimum placement strategies (in horizontal or vertical manner) can be developed further to reduce the critical global interconnect lengths.

III. Circuit Style

For logic and memory implementation in SN3D, CMOS circuit style with SN3D specific physical mapping scheme is used. In SN3D, doping occurs during wafer preparation stage, and the doping profile for silicon stack is n-n, p-p, n-n, p-p and so on; two consecutive silicon layers are doped n-type first and followed by two consecutive layers of p-type and vice versa. Our initial investigation revealed that this order of silicon layer doping allows maximum utilization of CC and CG features, and thus results in density gain when circuits are implemented. To map circuits to this underlying fabric, a key requirement is symmetric layout; for this purpose, a combination of pass transistors and complementary transistor-based logics are used for circuit implementations. Fig.3 presents a range of elementary logic gates implemented in SN3D and their corresponding schematics. The red dotted lines on schematics and physical layouts represent the corresponding signal flow paths as well as delineate the 3-D circuit folding/mapping scheme in the SN3D fabric. Fig.3A shows an inverter implemented in SN3D using adjacent p and n-type junction-less transistors together with CG, CC and HI features; CG and CC are used to connect transistors' common input and output connections respectively, and HI is placed appropriately for isolations. Similarly, 2-input NAND (Fig.3B) and 2-input NOR (Fig.3C) gates are implemented by optimally mapping the connectivity in the circuits to the compact features (CCs, CGs, and HBs), where inputs are common gated optimally, and other series, parallel and output connections are routed through common contacts (CCs), and HI is placed to isolate connections appropriately. The consecutive p-p-n-n layers adopted enable the effective mapping of CMOS circuits to 3-D nanowire stack, in addition, the device placement can be optimized based on the symmetry of the circuit.

Following the similar mapping scheme, pass-transistor based XOR (Fig.3D) and MUX (Fig.3E) logic gates are implemented to demonstrate the pass transistor logic in the SN3D fabric. To demonstrate the arithmetic circuits, Fig.4 shows the physical layout and corresponding circuit schematic for a full adder design in SN3D, where all fabric components are used for physical mapping. As shown in Fig.4, 10 (ten) transistors in circuit schematic are mapped efficiently to the 10 stacked nanowires utilizing all fabric features; the top 4 transistors in the adder layout (Fig.4) share a common gate with CG feature and so on. Nano-vias here are used for two purposes: (i) to provide connectivity required between non-consecutive devices (Fig.4), (ii) to bring the signals to top metal layers where input, output and inter-gate/inter-block routing is carried out (Fig.1G &2). It is worthwhile to note that HBs can also be used for inter-gate and inter-block routings within the fabric, which make the SN3D circuits more compact and reduce the metal interconnects required in upper metal layers. Fig.4 provides intuition for tremendous density benefits of SN3D based designs since 10 transistors are placed in the 2-D footprint of just one transistor.

In the above circuit implementations, transistor sizes are uniform, however, certain circuits might require transistors with asymmetric sizes i.e., different drive strength transistors. In SN3D fabric, we can achieve such multiple drive strength

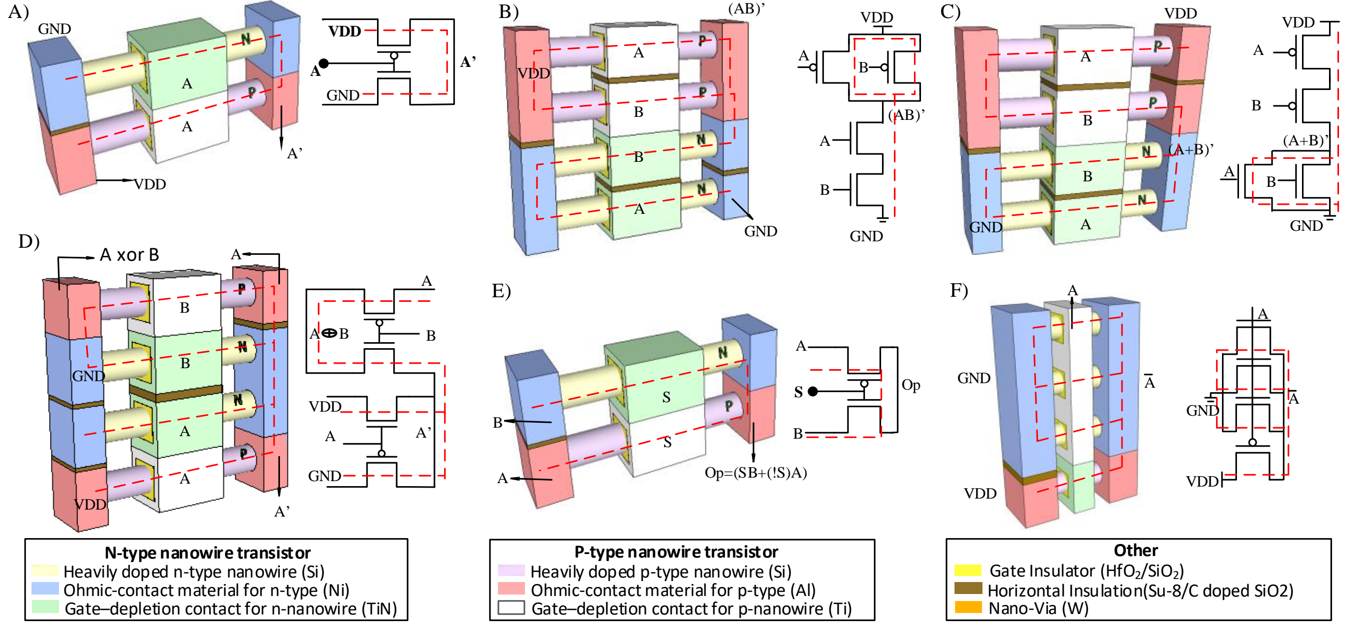

Fig. 3. Circuit implementation in SN3D. A) Inverter, B) 2-input NAND, C) 2-input NOR, D) 2-input XOR, E) 2:1 Multiplexer, F) Inverter (1:3) with 3x drive strength n-type and 1x p-type

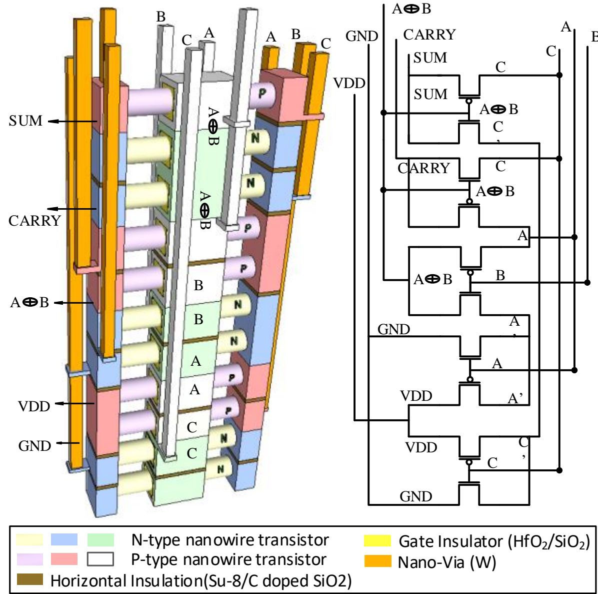

Fig. 4. 1-Bit Full adder schematic and SN3D layout

transistors by the parallel combination of adjacent nanowires using CG and CC features in a vertical or horizontal manner. Fig.3F depicts an inverter circuit with different n-type (3x) and p-type (1x) drive strengths, here, three parallel-connected nanowires act as 3x drive strength transistor for n-type. Another example for asymmetric circuit is standard 6T SRAM cell. We have designed and benchmarked SN3D SRAM in [17], which demonstrates the memory circuit implementation in SN3D fabric.

Thanks to the stacked nanowire fabric in SN3D, it provides highest device and interconnect granularity in z-dimension than any other die stacking 3-D approaches (M3D) [18], hence, it could spur the vertical integration of VLSI circuits. In addition, SN3D scales better than M3D. This is due to scalability in this fabric is determined by the ability to stack more nanowires in a vertical manner, and primarily rely on material etch and deposition techniques that are more controllable in comparison to the extreme lithography dependent device-scaling paradigm of traditional M3D. In addition, due to the sequential joining of layers in M3D, high-temperature processing on top layer affects the bottom layer; consequently, this yields to variability and reliability issues. Moreover, M3D faces routing congestion, because the available interconnect resources should not only accommodate the increased circuitry of the stacked dies, they should also endure the routing blockages due to perforating inter-layer vias that aggravate the congestion problem. Besides that, the inter-layer vias perforating through the dies also demand an area overhead. In contrast, SN3D overcomes the above limitations and fundamental connectivity bottleneck in 3-D with its inherent device-interconnect-fabric architecture. Furthermore, Gate All Around (GAA) Junction-less nanowire transistors [19], which are active devices in SN3D, have been reported to be the ultimate scaling devices among Tri-gate and MOSFET family[20][21], and exhibit excellent electrostatic control over the channel region with minimal short channel effects even down to 3nm [22][23]. Therefore, SN3D shows promising potential and conforms to the ITRS projection [24] for future scaling, that is, the third era of scaling will be eventually achieved through stacking multiple transistors vertically. Thus, we next benchmark our stacked nanowire transistors' 3-D (SN3D) circuit implementations.

IV. Benchmarking

A. Design Rules and Methodology

A comprehensive methodology, from the material layer to system, was developed to evaluate the potential of SN3D vs. CMOS. Fig.5 summarizes the methodology followed to evaluated SN3D logic circuits. We first perform the TCAD simulation of Junction-less NW transistors, from simulation

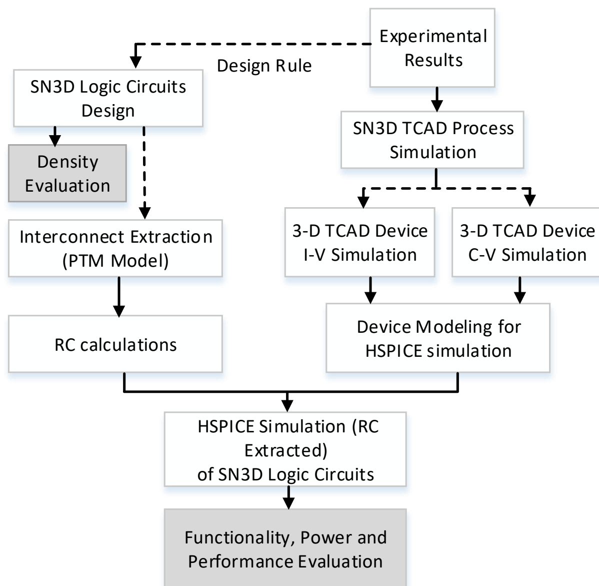

Fig. 5. Methodology for Benchmarking SN3D circuits

results we derive behavioral models for devices, which are later used for circuit design. For benchmarking, SN3D physical layouts directly give the area, whereas, power and performance are evaluated from RC extracted netlist of SN3D circuits. Next, we detail the steps.

Firstly, GAA Junction-less device behavior was characterized using 3-D TCAD Process and device simulations. Synopsys 3-D Sentaurus Process simulator was used to create the device structure emulating the actual process flow (discussed in Section. V); process parameters (e.g., implantation dosage, anneal temperature, etc.) used in this simulation were taken from our experimental work on Junction-less transistor [25] [26]. Fig. 6A depicts our process-simulated device; gate and contact materials labeled in the figure are chosen based on workfunction requirements [56] for the highly doped nanowire. 3-D Sentaurus Device [31] simulations were performed on this device to characterize the behavior, while considering nanoscale effects. The silicon nanowire band-structure and effect of band gap narrowing is calculated using Oldslotboom model [31]. The charge transport model employed to characterize the device current was hydrodynamic carrier transport model [31]; the model solves the Poisson and carrier continuity equations, lattice and carrier energy equations, and quantum transport model self consistently to determine the device current. The quantum transport model used to account for carriers quantum confinement in the nanowire channel was Density Gradient (DG) quantum correction model [31], which provides the most physically accurate results. Electron mobility (degradation) was modeled taking into account the effects of high-dopant, surface and interface scatterings, as well as velocity saturation. For circuit simulations, the TCAD simulated device characteristics were used to generate an HSPICE compatible behavioral device model. Regression analysis was performed on the device characteristics, and multivariate polynomial fits were extracted using DataFit software [32]. Mathematical expressions were derived to express the drain current as a function of two independent variables, Gate-Source (V_{GS}) and Drain-Source (V_{DS}) voltages.

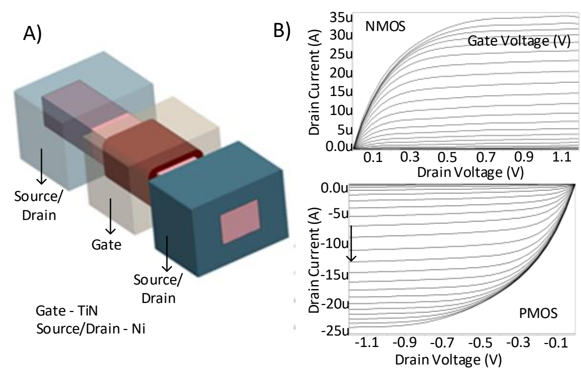

Fig. 6. TCAD simulation of junction-less nanowire transistor A) 3-D S process simulated device B) Drain current characteristics curves of n-type and p-type nanowire transistor modeled

These expressions were then incorporated into sub-circuit definitions for voltage-controlled resistors in HSPICE. Capacitance data from TCAD simulations was directly integrated into HSPICE using voltage-controlled capacitance (VCCAP) elements and a piece-wise linear approximation. The regression fits for current together with the piece-wise linear model for capacitances and sub-circuits define the behavioral HSPICE model for the V-GAA Junction-less transistor. Fig. 6B depicts drain current characteristic with respect to Vds and Vgs for n-type and p-type nanowire transistors modeled. The ON and OFF currents are 17.8µA and 0.1nA, and 17µA and 0.76nA for n-type and p-type respectively. The behavioral models' currents comply with the Sentaurus data accurately, within 5% error.

In addition, for accurate device characteristics, SN3D circuit simulations also accounted for 3-D layout specific interconnect parasitics and coupling noise effects considering actual

TABLE 1
SN3D DESIGN RULES

	Width - Z (nm)	Length - X (nm)	Thickness - Y (nm)	Spacing
Transistor Channel	16(2λ)	16(2λ)	16(2λ)	39
Transistor Spacing	-	-	-	23
Gate Electrode	32(4λ)	16(2λ)	34	-
Ohmic contacts	32(4λ)	24(3λ)	34	20
Bridge	24(3λ)	-	20	20
Horizontal Insulation	32(4 λ)	24 (3 λ)	5	-

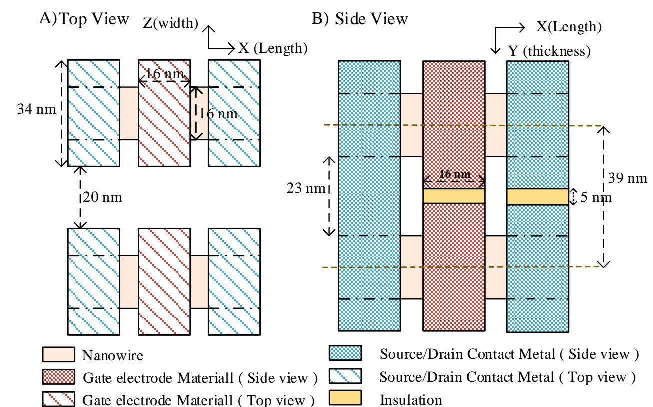

Fig.7. Design Rules for SN3D layout A) Top view B) Side view

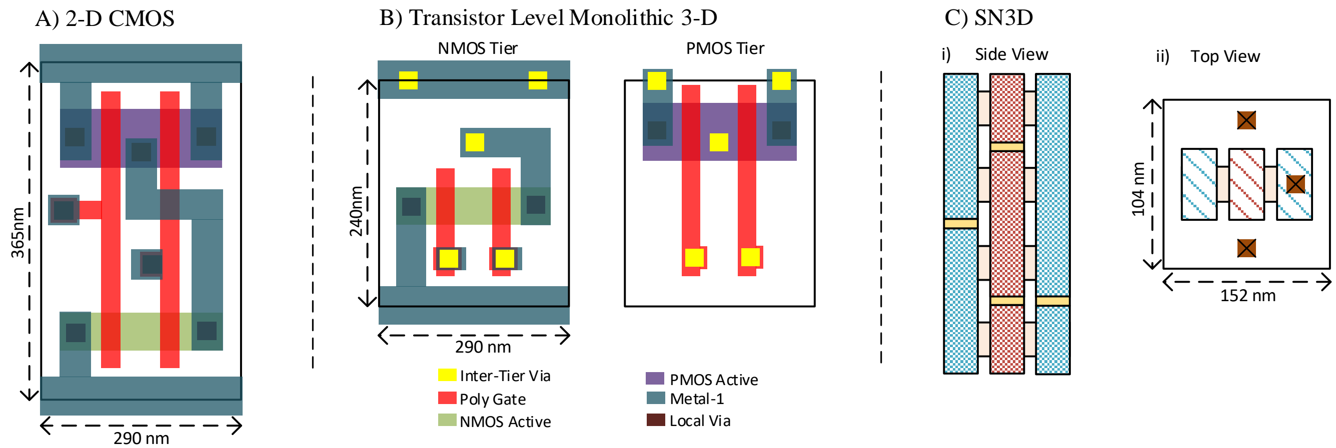

Fig.8.NAND layouts, A) 2-D CMOS layout, B) Side-view of SN3D NAND layout C) Top view

dimensions and material choices. Circuit mapping into SN3D fabric and interconnections were according to manufacturing flow (Section V) and followed fabric's design rules given in Table.1 (λ-based). SN3D needs 3-dimensional design rules—width (Z-axis), length (X-axis) and thickness (Y-axis) —listed in Table.1 and depicted in Fig.7. The top-view (Fig.7A) and side-view (Fig.7B) figures delineate these design rules at 16nm node. To mention few, the transistor (nanowire) channel dimensions for length x width x thickness are 16x16x16 nm (Fig.7A & 7B). Transistor channel spacing represents nanowire pitch in vertical (Y) direction, which is 39nm, while transistor spacing is 23nm (Fig.7B). Similarly, the dimensions for Gate electrode, ohmic contacts, HIs, and HBs are given in the Table.1 and accordingly represented in Fig.7. SN3D layouts in 3-D are constructed following these design rules.

The design rules formulated are assumed to be scalable with λ, this assumption validates based on following reasons. In addition to the dependence of scalability on shrinkage of nanowires, it also depends on the factors like number of nanowire layers that can be stacked and density of the stacks. Although in isolation, the pathways to achieve these are present, the nanowire strands ranging from 1 to 12 were demonstrated [15][36], large-scale top-down fabrications of nanowires were reported in [15][41], and GAA junction-less transistors were shown to scale down to 3 nm while performing reliably [20-23]. Our group has also demonstrated previously nanowire 3-D structures similar to SN3D [25][26]. Besides that, high aspect ratio nanowire (vertical) process techniques demonstrated in [46] [47] could also be employed for SN3D. Therefore, inferring from above demonstrations, the scalability in SN3D should be more aggressive than planar CMOS. However, the maximum number of nanowire layers stackable would be derivable only from SN3D specific fabrication experiments, and thus the benefits achievable would be constrained by vertical stackability.

B. *Benchmarking Results*

To investigate the benefits of SN3D, we have benchmarked the SN3D circuit layouts with respect to 2-D CMOS and M3D circuit layouts. We have designed range of elementary logic gates and a full adder circuit in SN3D, M3D and 2-D CMOS approaches, evaluated and compared their area, power and performance. Fig.6 elucidates NAND gate layouts in 2-D CMOS, M3D, and SN3D. For M3D implementation, the 2-D layout is split into pmos-tier and nmos-tiers with pmos and nmos devices respectively i.e., stacked dies (Fig. 2B). The area is calculated directly from the respective layout foot-prints. It can be noticed from Fig. 8 that the planar layout and M3D requires an area of 365x290 nm^2, and 240x290 nm^2 respectively, whereas SN3D NAND requires only 152x104 nm^2 which shows 6x and 4x area improvement, density saving increases with large circuits. Similarly, the area is estimated for different elementary gates and full adder in SN3D. RCs for SN3D, M3D, and 2-D CMOS physical layouts are estimated using Predictive Technology Modeling (PTM) [51], which are then incorporated into HSPICE circuit netlists to evaluate for functionality, power and performance. Table. 2 shows the area, power, and delays calculated for 2-input NAND, 1-bit full adder and 4-bit adder in 2-D CMOS, M3D, and SN3D respectively. With 10 stacked layers in SN3D fabric, our initial simulations and circuit evaluation results show the benefits of 11x, 19%, 18% and 6.7x, 8.69%, 9% over the state-of-art 2-D CMOS and M3D in terms of density, power, and performance respectively. We also performed the simulations for 4-bit adder at 22nm and 45nm. For these, the interconnects for SN3D are scaled according to λ-based design rules (Table. 1), whereas, interconnects for 2-D CMOS and M3D are scaled according to design rules given in [53]. Consequently, separate RCs are extracted at each node (16nm, 22nm and 45nm) in three cases, which are incorporated into HSPICE netlists, and simulated for power and performance. Table. 3 shows the comparison of the metrics, area, power and delay for 4-bit adder designs in 2-D CMOS, M3D, and SN3D at 16nm, 22n, and 45nm nodes, the benefits remain similar. Finally, 3-D ICs suffer from thermal challenges, however, because of the intrinsic heat extraction features the temperature of SN3D IC can be subdued. Our Finite Element Modeling (FEM) based simulation and analyses [54] show that the maximum temperature SN3D and M3D NAND structures reach are 314K and 340K respectively (Table.2). Since the temperature reduction of SN3D over M3D compared to baseline temperature is 65%, SN3D IC performs thermally far superior to M3D. Moreover, the temperature can be further brought down by employing the special heat extraction features at nanoscale, thus, the temperature in SN3D can be maintained around nominal operating temperature of ICs (~310K).

TABLE 2
AREA-POWER-DELAY AND TEMPERATURE COMPARISONS

	2-D CMOS			Monolithic 3-D CMOS			SN3D		
	Area (μm^2)	Power (W)	Delay (ps)	Area (μm^2)	Power (W)	Delay (ps)	Area (μm^2)	Power (W)	Delay (ps)
2-In NAND	0.104	3.3n	40.880	0.069	3.1n	37.55	0.015	2.83n	31.3
Full Adder	0.14	1.12u	248.5	0.093	1.13u	211	0.031	977.1n	191.2
4 Bit Adder	0.62	2.66u	938.1	0.38	2.3u	834	0.056	2.1u	767.4
Maximum temperature of 3-D NAND structure				340K			314K		
The base-line (ambient/substrate) temperature assumed in FEM simulations is 300K									

TABLE 3
AREA-POWER-DELAY COMPARISONS OF 4-BIT ADDER AT 16NM, 22NM AND 45NM

	2-D CMOS			Monolithic 3-D CMOS			SN3D		
	Area (μm^2)	Power (W)	Delay (ps)	Area (μm^2)	Power (W)	Delay (ps)	Area (μm^2)	Power (W)	Delay (ps)
16nm node	0.62	2.66u	938.1	0.38	2.3u	834	0.056	2.1u	767.4
22nm node	1.30	2.92u	1022.5	.796	2.52u	910.02	.156	2.3u	807.8
45 nm node	3.64	10.41u	1144.48	2.23	8.99u	1018.5	4.36	8.2u	936.2

V. MANUFACTURING PATHWAY

Manufacturing pathway presented in this paper is based on our previous experimental demonstration [25][26] and also demonstrations by other groups on stacked horizontal nanowires [14-16][33-36][38-41]. The manufacturing pathway for fabric assembly is composed of two stages. First the formation of stacked horizontal nanowires (Fig. 9B) using top-down fabrication techniques–lithographic patterning and material removal methods; next, the formation of fabric interconnects (Fig. 9D-9N) through thin-film depositions–sequential bottom-up material deposition and etch steps. We next discuss, major top-down fabrication pathways available to fabricate stacked suspended nanowires (as shown in Fig. 9B) from the bulk semiconductor substrate. One approach is successive anisotropic and isotropic plasma etching method [33]. Initially, a protruding Si ridge is formed through anisotropic etching, whose sidewalls are then passivated, followed by isotropic etching of Si underneath to realize free-held nanowire, and then, this process is continued to realize subsequent layers. Another approach is through combination of three techniques: Deep Reactive Ion Etching (RIE), self-limiting-thermal-oxidation [34][35] or wet oxidation [36], and isotropic etching. Here, initially a tall scallop patterned Si ridge is formed using BOSCH process i.e., deep RIE. Later, to isolate Si nanowires on scallop patterns, it can be either subject to self-limiting thermal oxidation [34][35] or wet oxidation [36]. The oxide (SiO_2) formed is then isotropically etched to realize stacked suspended nanowires. Alternate method reported in the literature is through "silicon-on-nothing (SON) process" [37][38-40]; initially, epitaxial layers of Si/SiGe are grown, followed by an anisotropic etching of Si, and selective isotropic etching of SiGe to realize free-held nanowire. This process is continued to form subsequent nanowires, where number of nanowires stackable is equivalent to the number of Si/SiGe layers grown [15]. Likewise, different demonstrations are available in nanowire fabrication literature that could be faithfully employed to realize SN3D. Dense arrays of stacked nanowires with stacks up to 13 were demonstrated [15][36][41]. Fabrication of sub-10nm nanowire transistors were reported [42-45] with excellent performance. Besides that, high aspect ratio (up to 1000[48]) vertical silicon nanowires are also demonstrated using different top-down approaches[46-48], similar methods could be employed to realize high aspect ratio vertical silicon ridges required in SN3D, from which stacked nanowires could be isolated [33-36]. In addition, our prior demonstration of deposition based fabric interconnect structures on vertical silicon nanowires [25][26] and also nanowires' gate/contact deposition methods in [14][15][36] establish the feasibility of SN3D fabric-interconnects. A full experimental demonstration of working prototype is beyond the scope of this paper and is currently work under progress. Nevertheless, a step-by-step TCAD emulation of manufacturing flow is presented showing the feasibility of proposed fabric.

Envisioned key process steps for SN3D fabric assembly are shown in Fig. 9. The manufacturing flow in Fig. 9 shows fabrication of a 2-input NAND gate in SN3D and was derived using Sentaurus TCAD Process Simulator [21] emulating actual manufacturing process flow. Stacked nanowire formation is the first step in fabric assembly. These nanowires are formed from a wafer that contains alternating doped Silicon and sacrificial SiGe layers (Fig. 9A). During wafer preparation, the SiGe and Si layers can be grown using reduced pressure CVD. The doping order we follow, that is, p-p-n-n and so on, provides efficient mapping for CMOS circuits. Later, defining a

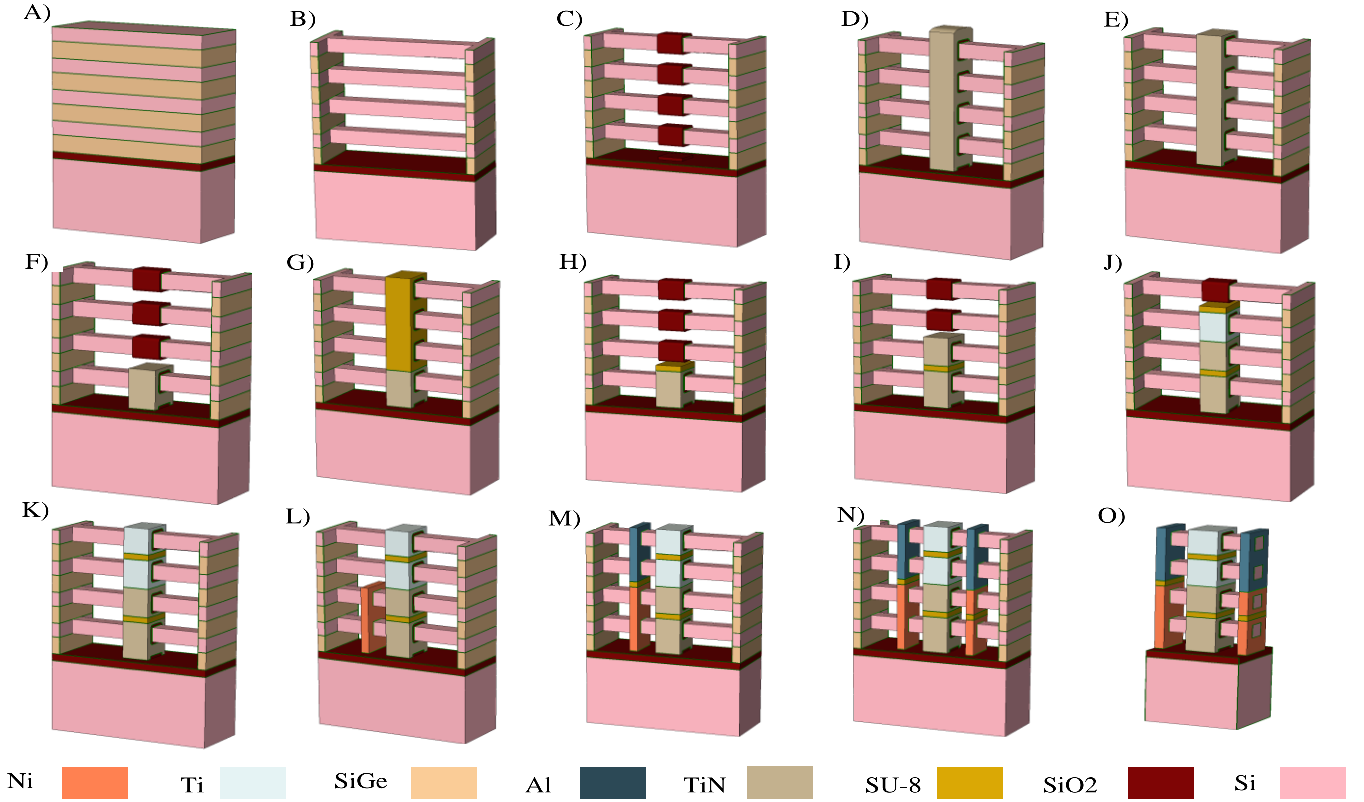

Fig. 9. Demonstration of proposed manufacturing flow through 3-D TCAD Sentaurus Process simulations of SN3D NAND structure: (A) Wafer preparation with sequential Si/SiGe layers on SOI substrate, bottom two layers n doped and top two layers are p doped; (B) suspended nanowires formation (W=10nm, L=200nm, Z=10nm) through etching sacrificial SiGe; (C) oxidation (3nm) of select region for transistors gate dielectric formation (L=16nm); (D) Gate material deposition and overfill; (E) planarization on top using Chemical Mechanical Polishing – CMP (other planarization techniques using self-planarizing materials are applicable as well); (F) Etch back, (G-H) overfill, planarization and etch-back of insulator material to form HI feature; (I) Second nanowire Gate formation through Deposition Planarization Etch-back (DPE) steps; (J) CG formation between second and third nanowires, and HI feature on top (DPE steps are performed using Gate and HI material); (K) top gate formation through DPE; (L) CC formation for n-type nanowires using DPE of ohmic contact material (left); (M) DPE to form HI, and CC for p nanowires using the corresponding ohmic material, thus HI separates the n and p nanowires' CC contacts; N) DPE steps on right side of the nanowires, forming, ohmic-contact for bottom n nanowire, HI, and long CC (NAND output node) for second, third, and fourth nanowires with corresponding ohmic-contact materials; O) removal of support structures and protruding nanowire overhangs.

nanowire pattern using hard mask, Si and SiGe on both sides of the pattern are anisotropically etched away forming nanowires with SiGe underneath, and deep trenches on both sides. Afterwards, the SiGe underneath is isotropically etched to realize stacked suspended nanowires as shown in Fig. 9B. Next step in the fabric assembly is gate oxidation (Fig 9C), which can be done through either thermal oxidation process (for SiO_2) or Atomic Layer Deposition (ALD) (for HfO_2), and it is followed by Gate material deposition (Fig. 9D). For p and n-type transistors, Ti and TiN will be used respectively as Gate materials. Thin layer of Gate material depositions can result in uneven surface at the bottom. For surface planarization, we propose two approaches: (i) overfilling of Gate materials, CMP planarization and controlled wet etching to obtain smooth surface as depicted in Figs 9D & 9E, or (ii) deposition and overfilling of all features by an insulating self-planarizing material, and controlled etch-back. Now the gate material is etched back to bottom nanowire (Fig. 9F). For insulating gate contact of bottom two nanowires, insulation material is deposited, planarized and etched back as shown in Fig. 9G & 9H. Next, Fig. 9I-9K show the Deposition-planarization-Etch back (DPE) of gate contacts, CGs and HIs for gate regions of the nanowires. Realization of subsequent Source/Drain contacts, CCs, and HIs follow a similar sequence of process steps: DPE as shown in Fig. 9L-9N. Contact materials for p and n-type nanowires are Nickel and Aluminum respectively. The support pillars on both sides are etched away to achieve final 3-D circuit structure as in Fig. 9O.

Lastly, the major obstacles SN3D face are the ones that are usually associated with adopting a new technology. SN3D is a significant departure from 2-D CMOS; hence, the circuit design, process flow, integration aspects are different. As discussed, the process steps that are different in SN3D are: Deep Reactive Ion (DRI) etching of nanowires, sequential bottom-up material deposit-etch steps, thin and precise isolation (HI) through ALD etc. Although these steps were shown in isolation by different groups including ourselves, the whole flow was not demonstrated for a fabric like SN3D. However, our prior work[49][50], experimental demonstrations [25][26] and similar work in literature [52][15][36] mitigate the risk.

VI. CONCLUSION

A new 3-D CMOS fabric for technology scaling is proposed in this paper. To prove the feasibility of proposed concept, we have derived key requirements for mapping circuits and evaluated a variety of circuits ranging from elementary gates to larger circuits such as 4-bit adder. Our initial projections reveal

tremendous benefits; for a 4-bit adder design, SN3D's benefits are 11x, 19%, 18% and 6.7x, 8.69%, 9% over state-of-art 2-D CMOS and transistor-level monolithic 3-D in terms of density, power, and performance respectively. The SN3D fabric shows huge potential for future 3-D integration, owing to the addition of third-dimensional attribute from device level to system level. Finally, to note, the proposed manufacturing techniques conform to existing practices in the industry and do not add any new manufacturing constraints

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